Register Number: …….

M.E. DEGREE EXAMINATIONS: MAY/JUNE 2010

Second Semester

APPLIED ELECTRONICS

ANE507: ASIC Design

Time: Three Hours **Maximum Marks: 100**

Answer All Questions

PART A (10 x 2 = 20 Marks)

1. What is manufacturing lead time?
2. Define Netlist.
3. What is Antifuse?
4. Compare CPLD and FPGA.
5. What is output stub?
6. What is the name of the interconnect bus in Xilinx EPLD?
7. In VHDL,explain the level sensitive process
8. What is target library?
9. What are the types of ‘stuck at’ faults?
10. What is reconvergent fanout?

PART B (5 x 16= 80 Marks)

11. (a) (i) Write short notes on ASIC design flow. (10)

(ii) Explain Latch operation with schematics. (6)

(OR)

(b) Describe the different types of ASIC with an example.

12. (a) (i) Explain Shannon’s Expansion theorem with an example. (10)

(ii) Draw and explain the Xilinx XC4000 configurable logic block. (6)

(OR)

(b) Explain the supply bounce and transmission line effects in AC output.

13. (a) Explain xilinx EPLD and Altera Max 5000 architectures with diagrams.

(OR)

(b) Discuss Electronic design interchange format.

14. (a) (i) Explain the sequential logic circuits using VHDL with an example. (10)

(ii) Write short notes on logic synthesis. (6)

(OR)

(b)(i)Explain combinational logic synthesis in VHDL. (10)

(ii)Discuss the working of a logic synthesizer. (6)

15. (a) (i)Explain the Basic ATPG algorithm. (10)

(ii)Write short notes on D-Calculus. (6)

(OR)

(b) Explain fault simulation in detail with different algorithms.

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