Register Number……...

M.E. DEGREE EXAMINATIONS: APRIL 2010

Second Semester

APPLIED ELECTRONICS

P07AE202 Computer Architecture and Parallel Processing

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (10 x 2 = 20 Marks)

1. Distinguish between hardware and software parallelism.
2. Define the term Latency with respect to program partitioning and scheduling.
3. Define Hit ratio.
4. What is a vector processor?
5. Define greedy cycle.
6. Define hot spot problem with an example.
7. List out the vector instructions available for vector machines.
8. What is a pipnet?
9. Define Multiprocessing.
10. Compare Static and dynamic scheduling.

PART B (5 x 16 = 80 Marks)

11. a) Explain with a neat diagram the architecture of Vector Supercomputer.

(OR)

b) Write in detail about the conditions of Parallelism.

12. a) Compare the characteristics of the CISC and RISC processors.

(OR)

b) Explain in detail the memory hierarchy technology and properties related to memory.

13. a) Write short notes on message passing mechanisms.

(OR)

b) Briefly explain about the Linear pipeline processors.

14. a) Explain the pipeline chaining on Cray supercomputers for the execution of the below given expression $Y(1:N) = S \times X(1:N) + Y(1:N)$

(OR)

b) Write about multiple context processors.

15. a) Explain in detail any two of the parallel programming models

(OR)

b) Describe the working of master slave kernels and floating executive kernels with reference to multithreaded UNIX.

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