Register Number (_____)

B.E DEGREE EXAMINATIONS Nov / Dec 2009

III SEMESTER

BRANCH MCE

U07MH303 & Digital Electronics

Time : Three Hours **Maximum Marks : 100**

Answer ALL Questions: -

PART A (10 X 1 = 10 Marks)

1. A K-map of five Variable will have _____ cells.

   a) 64 b) 28 c) 32 d) 31

2. Gray code is _____ code.
   a) Weighted code b) Non Weighted code c) Reflective d) Sequential

3. A decoder with 64 output line has _____ select lines.
   a) 5 b) 6 c) 4 d) 8

4. In a 4 bit parallel adder each full adder is considered to have a propagation delay of 30 ns then S_3 (MSB) will reach _____ time.

   a) 120 ns b) 120 ps c) 120 & d) 120ms.

5. Refresh circuit require for _____ RAM
   a) Dynamic b) Static c) Volatile d) Non-Volatile

6. In which flip-flop race around condition will take place?
   a) SR b) D c) T d) JK.

7. Hazard may occur in _____ circuits
   a) Synchronous Sequential b) Asynchronous sequential c) Combinational Circuit d) Transistor Circuit

8. A _____ occurs when an asynchronous circuit makes a transition through a series of unstable states.
   a) Non-critical race b) Critical race c) Cycles d) Races

9. The programmable array logic has programmable _____ gates and fixed _____ gates.

   a) NAND, NOR b) OR,AND c) AND, OR d) NOR,NAND

10. The output of the moor model is a function of
    a) Both the present state & input b) Only present state
    c) Both the next state & input d) Only next state

Answer ALL Questions: -
PART B (10 X 2 = 20 Marks)

11. Define redundancy theorem

12. What are the drawbacks of K-map method?

13. Implement the logic function $f = AB + \overline{A}\,\overline{B}$ using a suitable multiplexer.

14. What is meant by an "Essential-Prime-Implicant"?

15. Derive the characteristics of a D-flip flop.

16. What is a binary counter?

17. What is meant by critical race?

18. What are static 1 and static 0 hazards?

19. Define ASM chart ?

20. Draw the block diagram of meely and moore model of FSM.

PART C (5 X 14 = 70 Marks) (One Question from each unit)

21.a)(i) Simplify the boolean function F (A,B,C,D)= Σm(1,3,7,11,15)+$\sum$d (0,2,5). If don't care conditions are not taken care, what is the simplified boolean function? What are your comments on it? Implement both circuits .

ii) Implement $Y=(A+C)(\overline{A}+D)(A+\overline{B+C})$ using NOR gates only.

(OR)

b) What is the advantage of using tabulation method? Determine the prime implicants of the following function using tabulation method.

F(w,x,y,z) = Σ(1,4,6,7,8,9,10,11,15).

22 a) i)Implement the following function using with a (8:1) multiplexer.

F(a,b,c,d)= Σ(0,1,5,7,10,14,15) (8)

ii) Design a full Subtractor. (6)

(OR)

b). Design a network to convert 8421 BCD code to EX-3 code. (14)

23. a) i)Draw and explain 4-bit parallel in serial out shift register. (8)

ii) Design and explain the working of a synchronous mod-3 counter. (6)

(OR)

b). Design a synchronous counter for 4 → 6 →7 → 3 → 1 → 4 …… avoid lockout condition. Use JK type design. (14)

24 a) Find a static and dynamic hazard free realization for the following function using NAND gates and NOR gates.

F(a,b,c,d)= Σm(1,5,7,14,15)

(OR)

b) Develop the state diagram abd primitive flow table for a logic system thathas 2

inputs, x and y and output z and reduce primitive flow table. The behaviour of the circuit is stated as follows. Initially x=y=0. whenever x=1 and y=0 then z=1, whenever x=0 and y=1 then z=0. When x=y=0 or x=y=1 no change in z it remaind in the previous state. The logic system hqas edge triggered inputs without having a clock. The logic system changes state on the rising edge of the inputs. Static input values are not to have any effect in changing the z output.

25 a) Draw the ASMD charts for the following state transitions:

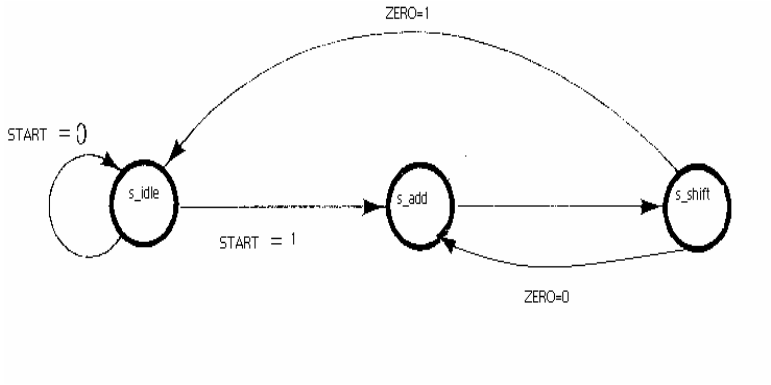
i) If x=1, control goes from state s1 to state s2: if x=0, generate a conditional operation R < =R+2 and go from s1+s2.

ii) If x=1, control goes from s1 to s2 and then to s3; if x=0 , R is cleared to xero and controlled goes from s1 to s3.

iii) State from state s1; then if xy=00,go to s2; if xy=10, go to s3; and if xy=01, go to s1; otherwise, go to s3.

(OR)

b) Design the control circuit of the binary multiplier specified by the state diagram of the fig shown below, using multiplexers, a decoder, and a register.



State Transition		**Register Operation**
From	To	
S_idle		Initial State
S_idle	S_add	A<=0,c<=0,p<=dp_width
S_add	S_shift	P<=p-1
S_shift		If(q [0])then (A<=A+B,C<=C_{out}) Shift right {CAQ}, C<=0.