Register Number……

**M.E. DEGREE EXAMINATIONS: DECEMBER 2009**

First Semester

**APPLIED ELECTRONICS**

ANE502: VLSI Design Techniques

**Time: Three Hours** **Maximum Marks: 100**

**Answer All the Questions:-**

**PART A (10 x 2 = 20 Marks)**

1. Define transistor gain factor.
2. What is channel length modulation?
3 Define noise Margin.
4. What is pass transistor?
5. What are the causes of static and dynamic power dissipation?
6. Define rise time and fall time.
7. What is the function of priority encoder?
8. What are the advantages of Elmore delay model?
9. What is fault sampling?
10. What is controllability?

**PART B (5 x 16 = 80 Marks)**

11. (a) Explain the working principle of nMOS Enhancement transistor with various modes of operations.

**(OR)**

(b) Explain DC equations and second order effects in MOS transistor.

12. (a) Explain the regions of DC characteristics of CMOS inverter.

**(OR)**

(b) Write short notes on:

(i) Super buffers (8)

(ii) Transmission gate (8)

13. (a) (i) Explain the behavior of the gate capacitance of a MOS device in the three regions of operations. (8)

(ii) Write notes on routing capacitance. (8)

**(OR)**

(b) (i) Explain about CMOS gate transistor sizing. (10)

(ii) Explain in detail about static power dissipation with neat diagrams. (6)

14. (a) Explain the following VLSI system Components:

(i) Multiplexers (8)

(ii) Comparators (8)

**(OR)**

(b) Explain about floor planning in VLSI Circuit.

15. (a) Briefly explain the system level test techniques with neat diagram.

**(OR)**

(b) Explain about fault models in CMOS technology.

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