Register Number: ……..

M.E. DEGREE EXAMINATIONS: JANUARY 2011

First Semester

COMPUTER SCIENCE AND ENGINEERING

CSE502: Advanced Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 2 = 20 Marks)

1. List and define the technologies critical to modern implementations?
2. Give the top 10 instructions for 80x86?
3. Define hazards with its classes?
4. What is the major limitation of the pipelining technique?
5. Mention the limitations in multiple issue processors?
6. What are the assumptions made for a perfect processor in the hardware speculation?
7. Define distributed shared memory?
8. How do you examine the performance of a memory consistent model?
9. Differentiate cache memory with virtual memory?
10. How I/O performance can be measured?

PART B (5 x 16 = 80 Marks)

11. a) (i) How do you measure the performance of a computer? Discuss in detail about the levels of the program used to evaluate the performance? [8]

(ii) Define Amdahl's law with a formula to calculate the overall speedup? Also mention the factors to find speed up using Amdahl's law? [8]

(OR)

b) With a neat table, explain in brief about the selection of addressing modes with its example, meaning and usage?

12. a) Define pipelining? Create a simple implementation for DLX and explain how it allows every instruction to be executed in 4 or 5 clock cycles with a neat diagram?

(OR)

b) Explain in detail about the common exceptions which vary across four different architectures?

13. a) Define instruction level parallelism? Discuss in detail about the limitations of ILP for related processors?

(OR)

b) What is multithreading? Explain in brief about how it uses ILP support to exploit thread level parallelism?

14. a) (i) Define multi processor cache coherence? Create a table for cache coherence problem for a single memory location (X), read and written by two processors (A and B)? [8]

(ii) Create a table which contains all possible messages with contents and function that is sent among the nodes to maintain coherence? [8]

(OR)

b) Write the code for the barrier using fetch-and-increment? Also assume that a fetch-and-increment operation takes 50 clock cycles. Determine the time for 20 processors to traverse the barrier. How many bus cycles are required?

15. a) How do you reduce cache miss penalty? Explain all the miss penalty reduction techniques in detail with an example for each?

(OR)

b) (i) Describe in detail about the different types of storage devices with a neat sketch? [8]

(ii) What is the average time to read or write a 512 byte sector for a typical disk? The advertised average seek time is 9ms, the transfer rate is 4MB/Sec, it rotates at 7200 RPM and the controller overhead is 1ms. Assume the disk is idle so that there is no queuing delay? [8]

****