Register Number: ……..

B.E DEGREE EXAMINATIONS: NOV / DEC 2010

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U07EC701: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:

PART A (10 x 1 =10 Marks)

1. In twin-tub process the electrical property of the layer depends on ----------

   a) Polysilicon b) Impurity c) Dopant and concentration of silicon d) Oxidation

2. Growth of thin layer of Silicon with controlled amount of impurities over the substrate is known as

   a) Photolithography b) Diffusion c) Epitaxy d) EBL

3. When a MOS device is in saturation, the effective channel length ---------- when Vds increases

   a) Increases b) Decreases c) Does not vary d) Varies randomly

4. Increase in threshold ----- ---------- circuits.

   a) leads to slower b) leads to faster c) does not effect d) Damages

5. Transmission gates degrades logic ----------

   a) Both 0 and 1 b) Neither 0 nor 1 c) Only 0 d) Only 1

6. Charging and discharging of load capacitor leads to ---------- power dissipation.

   a) High b) Low c) Static d) Dynamic

7. One of the programmable ASIC is

   a) PLD b) PLA c) PLC d) FPGA

8. In FPGA ---------- block provides the connection of internal CLB's with external packaged pins.

   a) Input b) Output c) I/O d) CLB

9. Which of the following best describes a UDP?

   a) A module which can have several outputs

   b) A combinational or sequential piece of logic described with truth table

   c) A module with variable parameters

   d) All of the above.

10. Which of the following is used for verilog-based synthesis tools?

a) Intra-statement delay statements can be synthesized, but inter-statement delays cannot

b) Inter-statement delay statements can be synthesized, but intra-statement delays cannot

c) Initial values on the wires are always ignored

d) Synthesized results are identical for ‘if’ and ‘case’ statements.

PART B (10 x 2 = 20 Marks)

11. Compare NMOS and PMOS devices.
12. State the features of BiCMOS technology.
13. List the electrical properties of MOS circuits.
14. Define pull up ratio.
15. Draw 2:1 MUX using transmission gate.
16. Distinguish between combinational and sequential circuits.
17. Mention the different types of programming structure available in PAL.
18. Give the application of PLA.
19. List five verilog gate primitives.
20. What is meant by continuous assessment statement in verlog HDL?

PART C (5 x 14 = 70 Marks)

21. a) (i) Draw and explain the P-well process in detail. (8)

(ii) Explain the twin tub process with neat diagram. (6)

(OR)

b) (i) Describe the BiCMOS fabrication in an n-well process. (8)

(ii) Compare CMOS and bipolar technologies. (6)

22. (a) (i) Obtain the pull up and pull-down ratio of NMOS inverter. (10)

(ii) Derive the transconductance of NMOS transistor. (4)

(OR)

(b) (i) Discuss the origin of latch-up problems in CMOS circuits with necessary diagrams. (10)

(ii) Draw the stick diagram of CMOS inverter. (4)

23. a) (i) Implement the following function using CMOS gates

$$f(A,B,C) = \overline{A}BC + A\overline{B}C + AB\overline{C}$$ (8)

(ii) Discuss the operation of CMOS latch. (6)

(OR)

b) (i) Describe the operation of a dynamic CMOS logic three input NAND gate. (8)

(ii) Explain the switch logic implementation of four-way multiplexer. (6)

24. a) (i) Describe the programmable logic structure available in PAL. (7)

(ii) Explain the finite state machine design using PLA. (7)

(OR)

b) Explain the FPGA design flow with neat diagram. Enumerate clearly the different steps involved.

25. a) (i) Write a verilog program for 3 to 8 decoder in gate level description. (10)

(ii) List the differences between behavioral and RTL modeling. (4)

(OR)

b) (i) Give a verilog structural gate level description of a bit comparator. (10)

(ii) Briefly describe the conditional statements available in verilog. (4)

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