Register Number: ……..

B.E DEGREE EXAMINATIONS: NOV / DEC 2010

Seventh Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

U07EI701: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:

PART A (10 x 1 =10 Marks)

1. Linear region is also called ---------- region where the drain current is dependent on the gate and the drain voltage w. r. to the substrate.

   a) Cut off b) saturation c) weak inversion d) Strong inversion

2. The threshold voltage V_T for a MOS transistor can be defined as the Voltage between ---------- terminals below which the drain to source current effectively drops to zero.

   a) gate and source b) Drain and source c) Drain and gate d) drain and source and gate.

3. The steady state power dissipation of the CMOS inverter circuit is

   a) High b) low c) moderate d) negligible.

4. Color code used for single poly silicon in nMOS Technology is

   a) Green b) Red c) Blue d) yellow

5. The complementary CMOS circuits have no static power dissipation, since the circuits are designed such that the pull-down and pull-up networks are ----------

   a) Mutually exclusive. b) Mutually inclusive c) internally connected d) externally connected.

6. A ratioed logic which uses a grounded pMOS load is referred to as a ----------gate

   a) pseudo-nMOS b) Dynamic CMOS c) Static CMOS d) clocked nMOS

7. FPGAs are quite different from CPLDs because FPGAs do not contain ----------

   a) Multiplexer b) Demultiplexer c) flip flop d) AND or OR planes.

8. The QFP package has pins on all ----------

   a) one side b)Two sides c) three sides d) four sides

9. Two or more subprogram to be executed in a same name, overloading of Subprogram should be performed. It is called as ----------

   a) Packages b) procedure c) subprogram over loading d) subprogram execution.

10. The output of a Moore finite state machine(FSM) depends only on the state and not on its

    a) Present & past outputs b) past outputs c) present state d) next state

PART B (10 x 2 = 20 Marks)

11. Give the expressions for drain current for different modes of operation of MOS transistor.
12. What is CMOS latch up? How it can be prevented?
13. What are stick diagrams?
14. Define a super buffer.
15. What is true single phase clocked register?
16. What are the major limitations associated with complementary CMOS Gate?
17. Define finite state machine.
18. What is the importance of the PLA/FSM in VLSI?
19. What are the different types of modeling VHDL?
20. Give two examples of FPGA devices.

PART C (5 x 14 =70 Marks)

21. a) Write the fabrication method of CMOS process and explain with neat diagram.

(OR)

b) (i) Drive the expression for the nMOS transistor current equation (8)
(ii) Explain the different regions of operations of MOS transistor. (6)

22. a) (i) Explain in detail about the operation of nMOS inverter. (7)
(ii) Explain the operation of Bi CMOS technology with neat diagram. (7)

(OR)

b) (i) Determine the pull up to pull down ratio in the nMOS circuit . (10)
(ii)Draw the stick diagram for the CMOS inverter. (4)

23. a) (i) Explain the operation of Barrel shifter with neat diagram. (7)
(ii) Write about Dynamic CMOS with relevant sketch. (7)

(OR)

b) (i) Give the NAND-NAND implementation $\gamma = ABC + DEF$ in stick form. (6)
(ii) Draw the static AOI CMOS gates to realize $\gamma = (AB + CD)$. (8)

24. a) (i) Draw the architecture of Xilinx FPGA and explain its operation. (7)
(ii) Explain different types of PLDs with examples. (7)

(OR)

b) (i)Explain the structure of MAX 7000 CPLD. (7)
(ii) Draw and explain the basic nMOS PLA structure. (7)

25. a) (i) Write a VHDL coding for the Decade counter. (7)
(ii) Write a test bench coding for the JK flip flop and T flip flop. (7)

(OR)

b) (i)Write a VHDL coding for the Multiplexer using structural modeling . (7)
(ii) Explain about RTL design and packages in the VHDL. (7)

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