Register Number: ………………

B.E DEGREE EXAMINATIONS: NOV/DEC 2010

Sixth Semester

ELECTRONICS AND COMMMUNICATION ENGINEEIRNG

U07EC604: Computer Architecture

Time: Three Hours   **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 1 = 10 Marks)

1. What is binary equivalent of -19 in 8 bit binary representation?

    (a) 11101100   (b) 11101101   (c) 11101110   (d) 11101111

2. A floating point number is normalized if

    (a) MSB of mantissa is zero   (b) MSB of mantissa is nonzero

    (c) LSB of mantissa is zero.   (d) LSB of mantissa is nonzero.

3. How many 4-bit adders are required to built a 16 bit carry look-ahead adder

    (a) 16   (b) 8   (c) 4   (d) 2

4. Booth algorithm is used for

    (a) Negative multipliers   (b) Positive multipliers

    (c) Negative and positive multipliers   (d) Unsigned multipliers

5. Cache memory is used for increasing the speed of

    (a) Address Bus   (b) Data Bus   (c) Clock Signal   (d) Processor

6. Multiprogramming is used to enable CPU to

    (a) Simultaneously process independent programs

    (b) Sequentially process independent programs

    (c) Identify different programming languages

    (d) Identify specific programming languages

7. Data hazards occur when

   (a) Data are corrupted   (b) Data are delayed   (c) Data are huge   (d) Data are coded

8. Multiphase clocking refers

   (a) Two or more clock signals

   (b) Two or more phase angles of single clock signal

   (c) Two or more amplitude levels of single clock signal.

   (d) Two or more speeds of single clock.

9. PCI interface is assigned an address in

   (a) Main memory   (b) Processor memory
   (c) Auxiliary memory   (d) Magnetic memory

10. Cycle stealing allow DMA controller to transfer
   (a) One data word at a time   (b) Two data word at a time
   (c) Three data word at a time   (d) Four word at a time.

PART B (10 x 2 = 20 Marks)

11. What is significance of 2's complement in digital logic?
12. Differentiate fixed point and floating point representations.
13. Draw binary addition –subtraction logic network diagram and clearly label it
14. What is bit pair recoding of multipliers?
15. Mention applications of RAM and ROM.
16. What are the functions of memory management unit?
17. What are steps for execution of an instruction for a processor?
18. What are branch instructions?
19. Give two differences between central computer and peripheral device.
20. What are memory-mapped I/Os and isolated I/Os?

PART   C   (5 x 14 = 70 Marks)

21. a) Draw a 4 bit combinational circuit shifter. Explain its operation with the help of functional table.

(OR)

  b) (i) Define arithmetic micro-operations and give their classifications.   (6)

    (ii) Explain a 4-bit binary incrementer with circuit diagram.   (8)

22. a) Draw a circuit diagram for binary restoring division and explain functioning of it with the help of an example and algorithm.

(OR)

  b) (i) Explain implementation of array multiplication of positive binary operands.   (10)

    (ii) Give IEEE floating point format for single precision.   (4)

23. a) Describe associative memory with block diagram. Explain read and write operation in respect of associative memory.

(OR)

  b) Illustrate concept of virtual memory and describe memory table for mapping a virtual address.

24. a) Explain multiple-bus organization giving example of three-bus organization of the data path.

(OR)

  b) What is the basic concept of instructions pipelining? Explain with the help of a 4-stage pipeline.

25. a) Explain asynchronous communication interface .Draw its block diagram and explain timing and control process.

(OR)

  b) What do you understand by Daisy-Chaining priority interrupts? Elaborate your answer with the help of examples and diagrams.

****