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B.E DEGREE EXAMINATONS: NOV/DEC 2010

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U07EC305: Electronic Circuits I

Time: Three Hours **Maximum Marks: 100**

Answer All Questions:-

PART A (10 x 1 = 10 Marks)

1. In a CE amplifier, thermal runaway is unconditionally avoided if V_{CE} is

   A) >Vcc/2 B) <Vcc/2 C) Vcc/2 D) $(Vcc/2)^{1/2}$

2. Which biasing circuit is not suitable for biasing MOSFET?

   A) Fixed Bias B) Self Bias C) Voltage Divider Bias D) Both A & C

3. Transistor amplifier configuration which simultaneously provides high current gain and high voltage gain is

   A) CB configuration B) CE configuration C) CC configuration D) All the above

4. The Darlington connection

   A) Increases input resistance B) Increases current gain

   C) Decreases current gain D) Increases voltage gain

5. The Miller input capacitance of an amplifier is a function of

   A) Input coupling capacitor B) Voltage gain

   C) Bypass capacitor D) Output coupling capacitor

6. In high frequency π model of CE transistor, capacitance C_e accounts for

   A) Excess minority carrier storage in base region B) Collector junction barrier capacitance

   C) Emitter junction barrier capacitance D) Both A & C

7. Maximum theoretical conversion efficiency of Class A transformer coupled amplifier is

   A) 15% B) 25% C) 50% D) 78.5%

8. For the Class A operation the Q point is to be located at

   A) Midpoint region B) Cut off region C) Below midpoint region D)above midpoint region

9. The ripple factor of a full wave rectifier is

   A) 0.482 B) 1.211 C) 0.287 D) 0.693

10. For a particular regulator the output voltage on no load is observed as 10 V while the full load output voltage is observed as 9.8 V. Find its load regulation.

    A) 15% B) 2% C) 19.8% D) 2.04%

PART B (10 x 2 = 20 Marks)

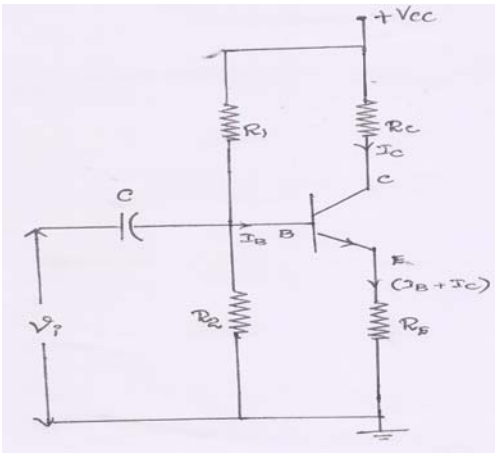
11. What is the significance of Q point?
12. Brief how the operating point can be made stable using Compensation technique.
13. State the dual of the Miller's theorem with the help of a circuit diagram.
14. List the methods for improving the CMMR.
15. Define gain bandwidth product.
16. What is the effect of internal transistor capacitances on the bandwidth of the amplifier?
17. Justify why frequency distortion is not significant in A.F. power amplifiers.
18. What is Heat Sink? State the function of it.
19. State a solution to overcome surge current.
20. Specify the necessity for the usage of Bleeder resistance R_B.

PART C (5 x 14 = 70 Marks)

21. (a) (i) Derive an expression for the stability factor S for CE amplifier with (a) Fixed Bias (b) Self Bias (8)

(ii) In the CE amplifier of figure I_E = 1 mA, R_E = 1000 Ω and β =49. Find the values of R_1 and R_2 such that the stability factor S does not exceed 5.

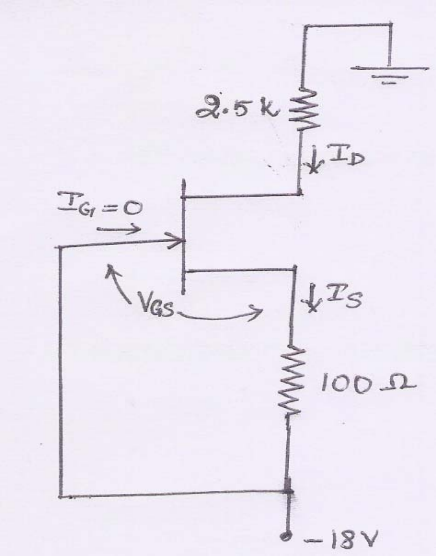
Assume Vcc = 5 volts and V_{BE} = 0, R_c = 1000 Ω (6)



(OR)

(b) (i) Explain how the biasing is carried out in Enhancement MOSFET and also State the reason why FET is used as VVR. (8)

(ii) The JFET shown in figure has I_{DSS} = 8 mA and V_p = -3V. Calculate the following parameters I_{DSQ}, V_{DSQ}, V_{GSQ} (6)



22. (a) (i) Draw the circuit of an emitter follower. Write the expression for its current gain, voltage gain, input resistance and output admittance using CE h-parameters. (10)

(ii) What is the effect of biasing circuit on the input impedance of an emitter follower? (4)

(OR)

(b) (i) With a neat sketch explain the Differential and Common mode operation of a Emitter coupled Differential amplifier. (10)

(ii) Can the Differential amplifier be used in modulator circuits? Justify the answer. (4)

23. (a) (i) Suggest the effects of coupling and bypass capacitor on the bandwidth of the amplifier (5)

(ii) Draw the circuit of a CS amplifier stage, also draw its small signal high frequency equivalent circuit and obtain the expression for high frequency (9)

(1) Voltage gain

(2) Input admittance

(3) Output admittance

(OR)

(b) (i) Derive an expression for overall upper and lower cut off frequency of multi stage amplifier. (7)

(ii) Write short notes on (7)

(1) Rise time

(2) Sag

24. (a) (i) Explain how cross over distortion is caused. Describe a method of reducing the cross over distortion. (8)

(ii) A complementary push-pull amplifier has capacitive coupled load $R_L = 8\Omega$, supply voltage = 12V. Calculate i) Pac max, ii) P_D of each transistor, iii) Efficiency. (6)

(OR)

(b) (i) Compare Direct coupled class A amplifier with the transformer coupled class A power amplifier. (6)

(ii) A single transistor amplifier with transformer coupled load produces Harmonic amplitudes in the output as

$B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA & $B_5 = 1$ mA

(A) Determine the percentage total harmonic distortion

(B) Assume a second identical transistor is used along with a suitable transformer to provide push pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion. (8)

25. (a) (i) A half wave rectifier feed a resistive load of 10 k Ω through a power transformer having a step down turns ratio of 8:1 and operated from 230 V, 50 Hz A.C. mains supply. Assume the forward resistance of the diode to be 40 Ω and transformer secondary winding resistance as 12 Ω. Calculate the maximum, RMS, and average values of current, DC output voltage and power, efficiency of rectification and ripple factor. (10)

(ii) Suggest the rectifier circuit to obtain the efficiency of 81.2% and also find the T.U.F of the same circuit (4)

(OR)

(b) (i) For L and π filter obtain the expression of ripple factor provided bridge rectified signal is applied as the input. (8)

(ii) With the neat sketch explain the operation of SMPS. (6)

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