Register Number: ……

**B.E DEGREE EXAMINATIONS: NOV/DEC 2010**

Third Semester

**ELECTRONICS AND COMMMUNICATION ENGINEEIRNG**

U07EC303: Digital Electronics

**Time: Three Hours** **Maximum Marks: 100**

**Answer ALL Questions:-**

**PART A (10 x 1 = 10 Marks)**

1. onvert $3643_8$ to hexadecimal

   A. $3A7_8$ B. $7A3_{16}$ C. $7A3_8$ D. $3A7_{16}$

2. Obtain the 9's complement of 7865

   A. 7548 B. 6421 C. 4321 D. 2134

3. The RTL family has

   A. poor noise immunity B. high average power dissipation

   C. speed of the operation is low D. All the above

4. The equation for the carry of an half adder is

   A. xy B. x′y′ C. x′y D. (xy)′

5. Determine the number of flip-flops that would be required to build the Mod-11

   A. 3 B. 4 C. 5 D. 6

6. ASM is used to represent

   A. Sequential Circuit & Combinational circuit

   B. Sequential Circuit

   C. Combinational circuit

   D. Neither Sequential Circuit nor Combinational circuit

7. In pulse mode circuits it is assumed such that

   A. Two pulses arrive at the same time B. No two pulses arrive at the same Time

   C. More than two pulses arrive at the same time D. Both A & B

8. If the output goes to state 0 when the output is expected to remain in state 1 as per the state analysis, the hazard of this nature is known as

   A. Static – 0 hazard B. Static – 0 hazard C. Essential hazard D.Dynamic hazard

9. How many 1024 x 1 RAM chips are needed to construct a 1024 x 8 memory system?

   A. 3 B. 4 C. 8 D. 6

10. How many address bits are needed to operate a 2K x 8 bit ROM memory?

    A. 10 address bits B. 4 address bits C. 8 address bits D. 11 address bits

## PART B (10 x 2 = 20 Marks)

11. Reduce the Boolean expression
    F = (AB′+AC′) (BC+BC′) (ABC)
12. Convert the following to other canonical form
    F(x, y, z) = π (0, 3, 6, 7)
13. Define Fan-in and Fan-out.
14. Implement the following function with a multiplexer.
    f (w, x, y) =Σ (0, 2 , 4, 6)
15. Differentiate level and edge triggering.
16. Distinguish Mealy, Moore models with ASM.
17. What do you mean by critical and non-critical races? How can they be avoided?
18. Compare fundamental and pulse mode asynchronous sequential circuits.
19. Differentiate ROM and RAM
20. Define the term mask programming.

## PART C (5 x 14 = 70 Marks)

21. a) (i) Using the K-map method , simplify the following expression and obtain their (9)

a) Minimum sum of product

b) Minimum product of sum

F (w, x, y, z) =Σ (0, 2, 5, 7, 9, 11, 13, 15, 16, 18, 21, 23, 25, 29, 31)

(ii) Obtain the canonical SOP and POS of the following expression

$f = x_1x_2x_3 + x_1x_3x_4 + x_1x_2x_4$ (5)

**(OR)**

b) (i) Simplify the Boolean expression using don't-care condition in SOP and POS (6)

F = w′ (x′y + x ′y′+ xyz) + x′z′ (y + w)

d = w′x (y′′z+ yz′) + wyz

(ii) Apply DeMorgan's theorem for the given expression (4)

F = ( (A′ + B + C+ D)′ + (A B′ C′ D)′ )′

(iii) Convert f = AB + B′CD into a product of maxterms by algebraic method. (4)

22. a) (i) Simplify the following function and implement it as (8)

A. Two level OR - AND gate network

B. Multilevel NOR – NOR network

f = Σ (0, 2, 3, 6, 8, 10, 11, 14, 15)

(ii) Compare TTL Logic with CMOS Logic. State the function of diode in the path of totem-pole output stage in a standard TTL gate? (6)

**(OR)**

b) (i) Design a circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that x = 1 if A = B and x = 0 if A not equal B. (7)

(ii) Design a BCD- to - excess-3 code converter with a BCD- to - Decimal decoder and 4 OR gates. (7)

23. a) (i) Realize D , JK, T flip flop using SR flip flop. (6)

(ii) Design a BCD counter with JK flip flops. (8)

**(OR)**

b) (i) Explain how ring and shift counters can be used as sequence generators. (7)

(ii) Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected. (7)

24. a) Design an asynchronous sequential circuit with 2 inputs $x_1$ and $x_2$ and with two outputs $Z_1$ and $Z_2$ for the following specifications.

i. When $x_1x_2 =$ 00 the output $Z_1Z_2 = 00$.

ii. When $x_1 = 0$ and $x_2$ changes from 0 to 1, the output $Z_1Z_2 = 10$

iii. When $x_2 = 1$ and $x_1$ changes from 0 to 1, the output $Z_1Z_2 = 01$

iv. Otherwise, the output is constant

**(OR)**

b) (i) How can the essential hazards be eliminated? (6)

(ii) Obtain the static hazard free asynchronous circuit for the following Function. (8)

$f = \Sigma (0, 2, 4, 5, 8, 10, 14)$

25. a) In detail explain the following

i. PLD

ii. FPGA architecture

**(OR)**

b) (i) Design a 4- bit Binary to Gray converters and obtain the simplified expression. (7)

(ii) Design a combinational circuit that accepts a 3 bit number as input and generates an output binary number equal to square of the input number using ROM. (7)

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