M.E. DEGREE EXAMINATIONS: NOV/DEC 2010
Third Semester
APPLIED ELECTRONICS
P07AEE11: Low Power VLSI Design

Time: Three Hours   **Maximum Marks: 100**
Answer ALL Questions:-
PART A (10 x 2 = 20 Marks)

1. Mention the basic principle of Low Power Design.
2. Define DIBL
3. Mention the two kinds of algorithm for transistor optimization.
4. List the characteristic features of static CMOS Logic.
5. List out the various methods for reducing the cross talk.
6. Draw the structure of four transistors DRAM Cell.
7. What is Gate Delay Model?
8. What is Power Sensitivity?
9. What are all the levels at which the improvement in power dissipation?
10. Define Behavioral level transforms.

PART B (5 x 16 =80 Marks)
11. a) Explain in detail about the Various limits in Low power VLSI Design
(OR)
    b) (i) With a neat Sketch ,describe the MIS Structure   (8)
       (ii) Discuss the various effects that influence the threshold voltage of MOSFET (8)

12. a) (i) Explain about Dynamic Differential Cascode Voltage switch logic.   (8)
       (ii) Explain about Enable/disable CMOS differential logic   (8)
(OR)
    b) (i) Explain the Combinational circuits technology independent optimization (8)
       (ii) Explain the pass transistor logic and implement the Full adder using SPL (8)
13. a) Explain in detail the Low power technique for SRAM with Diagram
(OR)
    b) Explain about the Low power Clock Design

14. a) (i) Explain in detail the Monte-Carlo Power Estimation   (8)
       (ii) Explain in detail the Advanced Sampling Techniques   (8)
(OR)
    b) Explain in details about Probabilistic Power analysis technique.

15. a) (i) Explain the optimization of power using operation Reduction   (8)
       (ii) Describe the software power estimation in detail   (8)
(OR)
    b) (i) Give the details about Automated low power code generation   (8)
       (ii) Explain in Detail of CO Design for low power.   (8)

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