B.E. DEGREE EXAMINATIONS: NOV/DEC 2010

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE105: Electronic Circuits I

Time: Three Hours   **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 1 = 10 Marks)

1. Why capacitive coupling is used to connect a signal to an amplifier?

  (a) To eliminate the noise   (b) to maintain constant biasing

  (c) to get better efficiency   (d) to improve gain of the amplifier.

2. Which is the most stable biasing circuit?

  (a) Fixed bias   (b) collector to base bias   (c) self bias   (d) voltage divider with Singh

     bias.

3. Which one of the following represents reverse voltage gain expression in CE amplifier?

  (a) $\dfrac{\Delta V_{be}}{\Delta I_b}$ (b) $\dfrac{\Delta I_c}{\Delta I_b}$ (c) $\dfrac{\Delta I_c}{\Delta V_{cc}}$ (d) $\dfrac{\Delta V_{be}}{\Delta V_{ce}}$

4. What is duty cycle?

  (a) $\dfrac{T_{ON}}{2T_{OFF}}$ (b) $\dfrac{T_{OFF}}{T_{ON}+T_{OFF}}$ (c) $\dfrac{T_{ON}}{T_{ON}+T_{OFF}}$ (d) $\dfrac{2T_{ON}}{T_{ON}+T_{OFF}}$

5. What is the output voltage V_o in voltage quardrupler when input voltage is V_{in}?

  (a) $V_o = 2 V_{in}$ (b) $V_o = 4 V_{in}$ (c) $V_o = \frac{1}{4} V_{in}$ (d) $V_o = 0.4 V_{in}$

6. Give the percentage of efficiency in class B Amplifier.

  (a) 78.5%   (b) 25% to 50%   (c) 95%   (d) 50% to 78.5%

7. Which power amplifier gives minimum distortion?

  (a) Class A   (b) Class B   (c) Class C   (d) Class AB

8. Which one of the following is not a type of SMPS?

  (a) step down switching regulator   (b) step up switching regulator

  (c) inverting switching regulator   (d) Non inverting switching regulator

9. In which region the transistor will operate to act as a switch?

  (a) Cut off   (b) Saturation   (c) Cut off & Saturation   (d) Active

10. What is the use of multistage amplifier?
    (a) To decrease the amplification   (b)To improve the efficiency
    (b) (c) For impedance matching
    (c) To remove the noise

PART B (10 x 2 =20 Marks)

11. What do you meant by thermal runway?
12. Write short notes on zero current drift in FET.
13. State Millers theorem.
14. Mention the advantages of h-parameters.
15. Define CMRR.
16. Define Sag in an amplifier?
17. Mention two conditions to be satisfied by a complementary symmetry power stage?
18. What is crossover distortion in a power amplifier and how to eliminate it?
19. Define transformer utilization factor (T.U.F)
20. What is meant by peak inverse voltage?

PART C (5 x 14 =70 Marks)

21. a) (i) Explain the common source self bias and voltage divider bias for FET.   (10)
        (ii) Show how a FET can be used as a VVR.   (4)
                                    (OR)
    b)   For the given circuit calculate V_E, V_B, I_B, V_{CE} and I_C, where $\beta = 100$ for the silicon
         transistor.
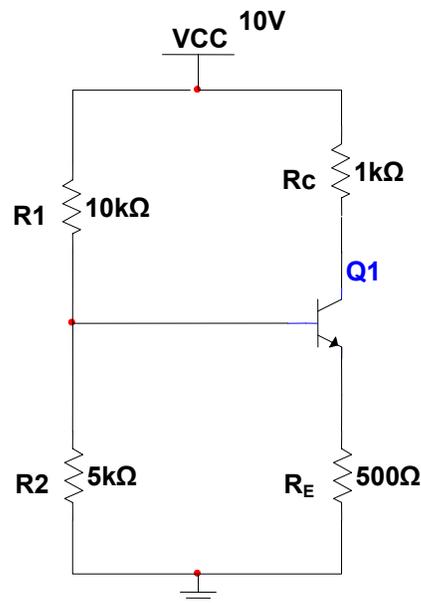
22. a) Draw the hybrid − π model for a common emitter transistor at high frequencies and
       derive the values of all the components interms of h − parameter.
                                    (OR)
    b) Explain about the common gate amplifier and derive its current gain, voltage gain, put
       impedance and output impedance expression.

23. a) Explain the working of emitter coupled differential amplifier with neat diagram.

(OR)

b) (i) Draw the cascode amplifier and explain in detail. (7)

(ii) Explain the method of improving CMRR. (7)

24. a) Explain in detail the operation of a class – B push pull power amplifier.

(OR)

b) (i) Briefly explain the use of heat sink in power amplifiers. (6)

(ii) Derive the expression for the power conversion efficiency of a class A power

plifier with resistive load. (8)

25. a) With necessary sketches explain the working of SMPS.

(OR)

b) (i) A half wave rectifier circuit is supplies from the 230V, 50Hz supply with a
transformer having step down ratio of 3:1 to a resistive load of 10 KΩ. The diode
forward resistance is 75 Ω, while transistor series resistance is 10 Ω. Calculate
maximum, average and RMS value of current. (10)

(ii) Design a simple zener regulator to give a DC fixed output of 5 volt upto a load
current of 50 mA. (4)

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