Register Number: ……

B.E/ B.TECH. DEGREE EXAMINATIONS: NOV/DEC 2010

Third Semester

ECE103: DIGIAL ELECTRONICS

(Common to Computer Science and Engineering, Electronics and Communication Engineering, Mechatronics Engineering and Information Technology)

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 1 = 10 Marks)

1. An inverted input AND gate is equivalent to

   A) NAND gate B) NOR gate C) NOT gate D) None of the above

2. What range of decimal values can be represented by a four digit hexadecimal number?

   A) 0 to 1024 B) 0 to 4096 C) 0 to 8192 D) 0 to 65535

3. What is the other name for Multiplexer?

   A) Data collector B) Data selector C) Data interpreter D) Data Distributor

4. What is the Odd and Even parity bit for a 3 bit message 110?

   A) 0 & 1 B) 1 & 0 C) 0 &0 D) 1 &1

5. The purpose of a clock input to a flipflop is to

   A) clear the device

   B) set the device

   C) always cause the output to change the states

   D) cause the output to assume a sate depending on the inputs

6. A synchronous Binary counter

   A) receives clock at flipflop representing LSB

   B) receives clock at first flipflop

   C) receives clock at all flipflops

   D) none of the above

7. Which of the following statement is correct with respect to a Mealy circuit?

   A) Input changes does not affect the output

   B) output is a function of present state as well as present input

   C) requires more number of states for implementing same function

   D) All the above

8. The unwanted switching transients that may appear at the output of a circuit is called as

A) switching characteristics B) output transients C) Indeterminate state D) Hazard

9. CMOS logic family uses only

A) MOSFET and resistor B) MOSFETs C) Bipolar Transistors D) NMOS devices

10. The Fan-in of a logic gate refers to the number of

A) input devices that can be connected B) input terminals

C) circuits that can be connected at the output D) output terminals

PART B (10 x 2 = 10 Marks)

11. Find the canonical SOP for the function f (x_1, x2, x3) = x_1' + x_2 x_3'
12. State Absorption & De-Morgan's law.
13. Distinguish between a multiplexer and a decoder.
14. Implement the function Y = AB' + A'B using only NOR gates.
15. What is Rise time and Fall time?
16. Give the truth table and excitation table for JK flipflop.
17. What is shift register and state its uses?
18. Classify Sequential logic circuit.
19. Define Noise Margin.
20. Draw the CMOS NOT gate circuit.

PART C (5 x 14 = 70 Marks)

21. a) (i) Plot the logical expression A'B'CD + AB'C'D + A'BC + AB' on a 4-variable K-map. Obtain the simplified POS expression from the map. (7)

(ii) Obtain the minimal SOP expression for the function.

Y= Σ m (1,5,7,13,14,15,17,18,21,22,25,29) + Σ d (6,9,16,23,30) (7)

(OR)

b) Simplify the following 5 variable Boolean expression using Quine McClusky Method.

F = ∑m (0,1,9,15,24,29,30) + d (8,11,31)

22. a) Design a 4 bit Comparator.

(OR)

b) Explain Half and full subtractor with truth table and logic circuit.

23. a) Explain the working of 4-bit synchronous counter with the help of timing diagram.

(OR)

b) Design a MOD 6 counter using JK flip flop. Write state table, reduce the expression using K – map and draw the logic diagram.

24. a) Design a sequential circuit with two D flip flops A and B and one input X.

When X = 0, the state of the circuit remains the same. When X = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

(OR)

b) Explain Static, Dynamic and essential hazards in digital circuit. Give Hazard free realization for the following Boolean expression.

$$F(A,B,C,D) = \Sigma m\ (1, 3, 6, 7, 13, 15)$$

25. a) (i) Classify the different IC logic families. (6)

(ii) Sketch the circuit of TTL NAND gate with two input terminals. Briefly explain the operation of the circuit. (8)

(OR)

b) (i) Design a combinational circuit using a ROM. The circuit accepts 3 bit binary number and generates its equivalent Excess 3 code. (7)

(ii) Implement the following functions using PLA. (7)

$$A(x, y, z) = \Sigma m\ (1, 2, 4, 6)$$
$$B(x, y, z) = \Sigma m\ (0, 1, 6, 7)$$
$$C(x, y, z) = \Sigma m\ (2, 6)$$

****