………………**M.E. DEGREE EXAMINATIONS: NOV/DEC 2010**Third Semester

APPLIED ELECTRONICS

ANE510: Low Power VLSI Design

Time: Three Hours   **Maximum Marks: 100**Answer ALL Questions:-PART A (10 x 2 = 20 Marks)

1. Why power dissipation has become the most critical factor in microelectronic technology?

2. What are the important sources of power dissipation in CMOS circuits.

3. State the equation for average power dissipation in CMOS. Also, what is the requirement for power estimation?

4. Define signal probability and signal activity.

5. What are the limitations of logic level low power optimization?

6. Compare transistor input reordering and transistor sizing methods?

7. Explain how divided word line architecture reduces power dissipation.

8. What is the advantage of 4T SRAM cell?

9. What is the main feature of higher level approach to software power optimization?

10. State the hardware-software co-design problem.

PART B (5 x 16 = 80 Marks)

11. a) (i) Obtain an expression for short circuit power dissipation of an unloaded CMOS inverter. (8)

    (ii) What are the limits of low power design? Explain. (8)

(OR)

  b) (i) Derive an expression for depth of depletion region for MIS structure. Use suitable assumptions. (8)

    (ii) What are the different capacitances that are present in a CMOS inverter? Illustrate how these factors affect the power dissipation. (8)

12 a) (i) State the equation for conditional probability of xi being '1' in the interval (t, t + T) while it does not switch at time 't'. What are the assumptions made? (8)

(ii) Given y = x1'x2x3 + x1x2'x3 +x1x2x3', determine a(y). Ignore simultaneous switching. (8)

(OR)

b) (i) Describe how switching activity is estimated in sequential circuits. What are the limitations of the assumptions made? (8)

(ii) Illustrate how BDD could be used in the signal probability computations. (8)

13. a) (i) Describe how FSM and combinational logic synthesis are used to reduce power dissipation. (16)

(OR)

b) (i) Explain how circuit level optimization for low power is achieved for CMOS gates. Use your own example. (16)

14. a) (i) Describe the generic organization of a SRAM cell. (8)

(ii) Illustrate how power reduction is carried out in sense amplifier circuits. (8)

(OR)

b) (i) Describe how voltage-swing reduction is effected in clock circuits. (8)

(ii) Explain special techniques that are used to reduce power dissipation in buses. (8)

15. a) (i) What are the advantages of using behavioral level transformations in power reduction? Explain with examples. (8)

(ii) Illustrate how algorithm level transformation could be used for reducing power in FIR filter. (8)

(OR)

b) (i) What are the requirements for instruction level power analysis technique? Illustrate how power reduction is achieved in instruction level power analysis. (8)

(ii) Describe co-design for low power in detail. (8)

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