………………**M.E. DEGREE EXAMINATIONS: NOV/DEC 2010**Third Semester

APPLIED ELECTRONICS

ANE511: DSP Integrated Circuits

Time: Three Hours   **Maximum Marks:**
100 Answer ALL Questions:-

PART A (10 x 2 = 20 Marks)

1. What is the main advantage of 2's complement representation?

2. Compare parallel and array multipliers.

3. State the important properties of discrete-time systems.

4. An FFT processor transfers input and output data a two 16-bit real numbers. If the I/O transfer frequency is 16 MHz, what is the time needed for transferring 1024 complex numbers?

5. What are the specifications for linear phase FIR filter. Draw a neat sketch.

6. 6. What is the necessity for multi-rate signal processing?

7. What are the major phases in the design of a DSP system?

8. State the equation for propagation delay in CMOS circuits.

9. What are the features of message based architectures?

10. What are the factors that limit the number of PEs in a shared memory system?

PART B (5 x 16 = 80 Marks)

11. a) (i) Illustrate the various fixed point representation formats with an example each.   (8)

   (ii) FFT algorithms require complex arithmetic. Design a suitable scheme for   (8)
       implementing complex multiplication. Justify the choice of processing elements used.

(OR)

   b) (i) Describe the various redundant number system representations. Illustrate how simple
       addition is carried out in each of these with an example each.   (8)

   (ii) Coefficients occupy huge memory in signal processing systems. Describe appropriate
       strategies that are used to reduce memory size requirements.   (8)

12. a) (i) Justify the large usage of discrete-time systems in general. Also, bring out the role of
       VLSI technology for advancement in digital signal processing systems.   (8)

   (ii) State the forward and inverse DCT equations. Describe how DCT is used in image
       processing systems.   (8)

(OR)

b) i) What are the factors that need to be considered while choosing an appropriate sampling frequency for a discrete-time system? Explain. (8)

(ii) The important design criteria is optimizing the adjustable filter coefficients. Describe how it is carried out for a typical adaptive system of your choice. (8)

13. a) (i) Using a schematic, explain the direct form structure for a linear phase FIR filter. (8)

(ii) State the important characteristics of FIR chips available commercially. (8)

(OR)

b) (i) Describe the salient features of any two analog low-pass filter approximations. (8)

(ii) What are the consequences of finite word length representation of coefficients and operand values? Describe each effect in detail. (8)

14. a) (i) What are the major steps in direct mapping approach in DSP system design? Illustrate with a flow chart. (8)

(ii) Trace the evolution of trends in CMOS technologies. Explain with respect to important parameters. (8)

(OR)

b) (i) Describe the various partitioning techniques used in DSP system design. (8)

(ii) Compare the different VLSI process technologies with respect to CMOS. (8)

15. a)(i) What are the main architectural components in ideal DSP design? Explain each of the constituent element in detail. (8)

(ii) A high throughput DSP system is required. Describe a suitable architecture for the same. (8)

(OR)

b) (i) Describe how large DSP systems are realized . Illustrate with respect to cascade and parallel forms of shared memory architecture.

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