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B.E DEGREE EXAMINATIONS: APRIL/MAY 2012

Fourth Semester

ECE103: DIGITAL ELECTRONICS

(Common to Electrical and Electronics Engineering & Electronics and Instrumentation

Engineering)

Time: Three Hours   **Maximum Marks: 100**

Answer All Questions:-

PART A (10 x 1 = 10 Marks)

1. In a signed binary numbers the sign bit is the

   a. Right most bit   b. Left most bit   c. Middle bit. d. Second bit.

2. An example for sequential code is

   a. 2421   b. 5211   c. Excess-3   d. 2422

3. Number of full adders required to construct n-bit serial adder are

   a. n   b. 1   c. n-1   d. 2n

4. The number of entries in 1 bit magnitude comparator is

   a. 4   b. 3   c. 2   d.5

5. T flip-flop is used as a

   a. Transfer data circuit   b. Toggle switch   c. Time delay circuit   d. As a switch

6. The number of flipflops required to count 0 to 63

   a.8   b. 6   c.10   d. 12

7. Shifting a binary data to the left by one bit position using shift register, amount to

   a. addition of 2   b. subtraction of 2   c. multiplication of 2   d. division of 2

8. In a Mealy circuit the output

   a. depends on present state of memory elements

   b. depends on present and past state of memory elements

   c. depends on present state of memory elements and also the External input

   d. depends on past state of memory elements

9. A PLA is a

   a. SSI device   b.LSI device   c.MSI device   d. VLSI device

10. Which of the logic family has the complementary outputs?

   a. DTL   b. IIL   c. TTL   d. ECL

PART B (10 x 2 = 20 Marks)

11. Convert $(634)_8$ to binary.

12. Prove that $A + \overline{A}B = A + B$.

13. Which gates are called as the universal gates? What are its advantages?

14. Define carry propagation delay.

15. Write the difference between level triggered and edge triggered flip-flops.

16. What is a master-slave flip-flop?

17. Implement the given function using 4:1 multiplexer $F = \sum m (0,1,2)$

18. What is asynchronous counter? Give an example.

19. Define Static RAM and dynamic RAM.

20. Distinguish between PLA and PAL.

PART C (5 x 14 = 70 Marks)

21. a) (i) Perform the subtraction 3571-2101 using

      (1) 10's complement   (2) 9's Complement.   (8)

    (ii) Express the following in decimal $(1011011)_2$, $(16)_{16}$ and $(165)_8$.   (6)

(OR)

  b) Simplify the following function using K-Map and Tabulation Methods.

      $F(A,B,C,D) = \sum m(0,1,5,7,8,9,10,11,14,15)$.

22. a) (i) Design a full adder using 8:1 multiplexer.   (6)

    (ii) Explain the half subtractor with truth table and reduce using Kmap and implement using only NOR gate.   (8)

(OR)

  b) Design a 4 bit binary to gray code converter and implement using X-OR gate.

23. a) (i) Explain the construction of clocked SR flipflop with truth table.   (10)

    (ii) Realize D flipflop using SR flipflop.   (4)

(OR)

  b) Design a MOD-7 synchronous counter using JK flip-flops. Construct a timing Diagram.

24. a) The circuit specified by the Flipflop equation

        $J_A = A$ $J_B = X'$, $K_A = AX'$ $K_B = A'X + AX'$ $Y = AB'$

Draw the logic diagram, write the state table and draw the state diagram.

(OR)

b) (i) Minimize the state table given below   (6)

Present state	Next state X(input)		Z(output)
	X=0	X=1	
A	A,0	B,0	
B	C,0	D,0	
C	A,0	D,0	
D	E,0	F,1	
E	A,0	F,1	
F	G,0	F,1	
G	A,0	F,1	

(ii) Explain the working of ring counter and write its applications.   (8)

25. a) (i) Explain Programmable Array Logic with a neat diagram.   (8)

(ii) Implement the following function using PLA

$F_1 = \Sigma\ m(1,2,4,6), F_2 = \Sigma\ m(0,1,6,7), F_3 = \Sigma\ m(2,6)$ (6)

(OR)

b) (i) Compare TTL,ECL and CMOS.   (7)

(ii) Explain the architecture of FPGA.   (7)

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