Register Number.....

M.E. DEGREE EXAMINATIONS: APRIL / MAY 2009

Third Semester

APPLIED ELECTRONICS

P07AEE05 – ASIC Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 x 1 = 20 Marks)

1) In _____ Layout the height of the cell is fixed but the width can vary.

A) Gate Array B) Standard Cell C) Macro Cell D) FPGA

2) Which of the following device has a Programmable AND array and a Fixed OR array?

A) PROM B) PLA C) PAL D) CPLD

3) _____ depends only on the load capacitance connected to the output of the logic cell and the input capacitance of the logic cell.

A) Electrical Effort B) Logical Effort C) Parasitic Delay D) Effort Delay

4) Propagate signal is obtained by _____

A) $A_i \bullet B_i$ B) $A_i + B_i$ C) $\overline{A_i \oplus B_i}$ D) $A_i \oplus B_i$

5) The basic logic cells in Actel ACT family of FPGA's are called _____

A) CLB's B) Logic Modules C) I/O blocks D) Interconnects

6) PAL22V10 has _____ number of macro cells

A) 22 B) 12 C) 10 D) 14

7) _____ logic cell contains 32 bit LUT, 2 D flip-flops and 9 multiplexers.

A) Actel ACT 1 B) Xilinx XC3000 C) Actel ACT 2 D) Xilinx XC4000

8) A CMOS inverter has _____ and _____

A) $V_{OH} = V_{DD}$ *and* $V_{OL} = V_{SS}$ B) $V_{OH} = V_{DD}$ *and* V_{OL} *is non – zero*

C) $V_{OH} = V_{DD} - V_{tn}$ *and* $V_{OL} = V_{SS}$ D) $V_{OH} = V_{DD} - V_{tn}$ *and* V_{OL} *is non – zero*

9) _____ interconnects in a Xilinx architecture join switch boxes.

A) Programmable B) Global C) General Purpose D) Direct

10) Transforming VHDL or Verilog code into a description of logic cells and interconnections is called as _____

A) Logic Synthesis B) Floor Planning C) Circuit Extraction D) Placement

11) _____ of a cell measures the driving capability of an output terminal.

A) Fan-in B) Fan-out C) Noise Margin D) PDP

12) EDIF stands for _____

A) Electronic Design Interchange Format B) Electronic Data Interchange Format

C) Electronic Design Information Format D) Electronic Data Information Format

13) _____ encoding sets one bit in a state register for each state.

A) Adjacent B) One-hot C) User Specified D) Moore

14) The maximal length sequence for PRBS generator having n flip-flops is _____

A) 2^n B) $2^n - 1$ C) 2^{n-1} D) $2^{n-1} - 1$

15) A fault that affects a larger portion of the circuit is called _____ fault.

A) hyperactive B) hard detected C) soft detected D) oscillatory

16) _____ is a Nondeterministic Fault Simulation.

A) Serial Fault simulation B) Parallel Fault simulation

C) Concurrent Fault simulation D) Probabilistic Fault simulation

17) _____ tool calculates the parasitic resistance and capacitance associated with each interconnect.

A) Circuit Extraction B) Synthesis C) Simulation D) Partitioning

18) There are _____ forms of SPF to describe the interconnect delay in Cadence.

A) 2 B) 3 C) 4 D) 5

19) _____ routing calculates the shortest path using tree or graph algorithms with the added restriction of using the available channels.

A) Sequential B) Hierarchical C) Order dependent D) Order independent

20) The limit of _____ of current per square micron of metal cross-section is good rule of thumb to follow for current density in a aluminum based interconnect.

A) 1 mA B) 10 mA C) 100 mA D) 1 μA

PART B (5 x 16 = 80 Marks)

21) a) i) Explain the structure of a 6 bit Wallace Tree multiplier (8)

ii) Discuss the sequence of steps involved to design an ASIC (8)

(OR)

21) b) i) Explain the various types of gate array based ASIC's. (8)

ii) Design a master slave D flip-flop and explain its working (8)

22) a) i) Explain the architecture of a Xilinx 3000 CLB (10)

ii) Write short notes on Static RAM (6)

(OR)

22) b) i) Discuss in detail about Logic Expanders (8)

ii) Compare the logic cells used by various programmable ASICs (8)

23) a) i) Compare and contrast the various types of Programmable ASIC interconnects. (8)

ii) Discuss the schematic design entry for ASIC (8)

(OR)

23) b) i) Discuss the various types of Low level Design languages. (10)

ii) Create a vectored instance of eight inverters inv0 through inv7. Write the netlist in internal and EDIF form and explain the contents. (6)

24) a) Explain in detail about Boundary Scan architecture.

(OR)

24) b) Explain D algorithm and PODEM algorithm with suitable examples.

25) a) i) Discuss a algorithm that solves the restricted channel routing problem. (8)

ii) Explain Lee Maze running algorithm for detailed routing. (8)

(OR)

25) b) Explain in detail about constructive placement and iterative placement.

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