# B.E. / B. TECH. DEGREE EXAMINATIONS: APRIL/MAY 2009

## Third Semester

## U07CS302 COMPUTER ARCHITECTURE

(Common to **Computer Science and Engineering** and **Information Technology** Branches)

**Time: Three Hours**                                        **Maximum Marks: 100**

### Answer ALL the Questions:-

### PART A (20 x 1= 20 Marks)

1. An instruction register is used to store

   A. The address of the next instruction to be fetched.
   B. The address of the data to be fetched
   C. The content at the memory location pointed out by the address register
   D. The content of the program counter.

2. LOAD ACCUMULATOR is a

   A. Zero address instruction
   B. One address instruction
   C. Two address instruction
   D. Three address instruction

3. The software responsible for the coordination of all the activities for the execution of a program is called

   A. Text editor        B. Operating system        C. Compiler        D. File system

4. The basic performance equation of any computing system, given T is the program execution time, N is the number of machine language instruction, S is the average number of basic steps needed to execute a machine instruction and R is the clock rate of the system , is of the form

   A. $T= N \times S / R$        B. $T= R \times S / N$        C. $R=N \times S /T$        D. $S= R \times N/T$

5. An unbiased technique used to truncate a floating point number to the closest approximation is
   A. Biasing        B. Rounding        C. Von Neumann Rounding        D. Chopping

6. A Register file is nothing but

   A. Accumulator                                    B. Block of memory locations
   C. All general purpose registers combined in a block        D. A single temporary register

7. What is the IEEE standard format for representing a floating point value

   A. 32-bit          B. 64-bit          C. 16-bit          D. 128-bit

8. The Bit-pair recording multiplication technique works by

   A. Doubling the maximum number of summands
   B. reducing the maximum number of summands into half
   C. Reduces the maximum number of summands by one third.
   D. Leaves the maximum number of summands unchanged

9. Operand forwarding avoids

   A. Structural hazards     B. Data hazards    C. Control hazards    D. Instruction hazards

10. Pentium-IV uses

    A. 7-stage pipeline     B.12-stage pipeline     C. 9-stage pipeline     D.20-stage pipeline

11. Bit-O-Ring technique is used to

    A. change the branch address              B. Perform Bit-wise OR operation
    C. Change the sequence counter            D. Change the content of Data register

12. A micro program counter is used to

    A. store the currently read control word
    B. read the data used by the control program
    C. read the control word sequentially from the control store
    D. store the control word

13. Memory cycle time is the time taken

    A. to write a memory location
    B. to read a memory location
    C. to complete a memory operation
    D. between the initiation of two successive memory operations

14. What is the time taken to refresh all rows of a 4K SDRAM at the clock rate of 133 MHz
    and suppose that it takes 4 clock cycles to access each row.

    A. 246 ms          B. 64 ms          C.16 ms          D.123 ms

15. The average access time in a computer having cache is given by the formula

    A. Average access time = Hit rate x Access time of cache + (1-Hit rate)x Miss penalty
    B. Average access time = (1-Hit rate)x Access time of cache+ Miss penalty
    C. Average access time= (1-Miss penalty)x Access time of cache
    D. Average access time = Hit rate x Miss penalty + Access time of cache

16. A disk unit has 20 recording surfaces, 15000 cylinders, 400 sectors/track and each sector has 512 bytes of data. The maximum number of bytes that can be stored in the unit is

    A. 40 GB      B. 60 GB      C. 20 GB      D. 80 GB

17. The routine executed in response to an interrupt request is called

    A. Device driver      B. Micro program
    C. Interrupt service routine      D. I/O subroutine

18. The mode in which the DMA controller is given the exclusive access to main memory is called

    A. Daisy chaining mode      B. Burst mode
    C. Direct mode      D. Cycle stealing mode

19. UART is a

    A. serial interface      B. parallel interface
    C. buffer      D. serial port device

20. The standard bus defined by the ANSI as X3.131 is

    A. PCI      B. RS-232      C. USB      D. SCSI

## PART-B (5 x 16= 80 marks)

21. (a).(i). Explain the basic operational concepts of the processor unit with a neat diagram showing the connections between the processor and the memory      (8)

    (ii). What is system software? Discuss in detail about various system software.      (8)

### (OR)

21. (b). Discuss in detail about various addressing modes with examples.

22. (a). Explain the working of a faster adder using carry look-ahead addition with a neat diagram.

### (OR)

22. (b) . (i) Explain the operation of Booth's multiplication algorithm.      (6)

    (ii) Multiply the following signed 2's complement numbers using Booth's algorithm. Multiplicand A= 110011 and multiplier B= 110110      (10)

23. (a) Explain the multiple- bus organization of data path inside a processor with a neat diagram.

(OR)

23. (b) (i) What are instruction hazards? What are the causes of instruction hazards (4)

(ii) Explain how branch penalty is reduced in conditional and unconditional branches.
(12)

24. (a) Explain Direct mapping and associative mapping in detail.

(OR)

24. (b) Explain virtual memory organization and address translation in detail.

25. (a) (i) Explain the DMA data transfer operation with a neat diagram. (8)

(ii) Discuss briefly about bus arbitration. (8)

(OR)

25. (b) (i) Explain how enabling and disabling of interrupts are done. (8)

(ii).Explain how multiple devices are handled using interrupts. (8)

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