Register Number.....

B.E. / B. TECH. DEGREE EXAMINATIONS: APRIL/MAY 2009

Third Semester

U07CS303 MICROPROCESSORS

(Common to **B.E. Computer Science and Engineering** and **B. Tech. Information Technology** Branches)

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 x 1= 20 Marks)

1. The number of address lines and data lines in 8085A microprocessor is

   a) 8 address lines 8 data Lines.
   b) 16 address lines 8 data Lines.
   c) 16 address lines 16 data Lines.
   d) 20 address lines 16 data Lines.

2. Program Status Word Refers to

   a) Accumulator and Flag Resister.
   b) Program Counter and Flag Register.
   c) Accumulator and Program Counter.
   d) Temporary register and Accumulator.

3. The number of Flag Register available in 8085A Microprocessor is

   a) 4 Flag registers. b) 5 Flag registers.
   c) 3 Flag registers. d) 2 Flag registers.

4. Program Counter is a

   a) 8 bit register. b) 16 bit register.
   c) 32 bit register. d) 4 bit register.

5. .The number of bytes required to store the instruction MOV C, A is

   a) 4 bytes. b) 3 bytes. c) 2 bytes. d) 1 byte.

6. 8085 has _____instruction sets

   a) 246 b) 256 c) 512 d) 521

7. The content of Accumulator after executing the instruction XRA A is

   a) 10101010 b) 00001111 c) 11110000 d) 00000000

8. MVI A,25
   CPI 25
   After executing the above mnemonics the status of Zero flag and carry flag are

   a) Z= 1 : C=0 b) Z= 0 : C=1 c) Z= 0 : C=0 d) Z= 1 : C=1

9. In 8085 Microprocessor the storage and retrieval of data on the stack should follow

a) First In First Out (FIFO)
b) Last In First Out (LIFO)
c) First In Last Out (FILO)
d) Last In Last Out (LILO)

10. 8085 microprocessor has ___ maskable interrupt

a) 6 b) 4 c) 2 d) 1

11. ____ has the highest priority among the interrupt signals

a) RST 7.5 b) RST 6.5 c) TRAP d) RST 5.5

12. The call location in hex for RST 0 is

a)0000 h b) 0008 h c)0010 h d)0018 h

13. DMA stands for

a) Decimal Multiplication Addition.
b) Direct Memory Access.
c) Direct Multiplication Access.
d) Direct memory addition.

14. 8255 IS

a) Programmable Peripheral Interface.
b) Programmable timer.
c) Programmable Interrupt controller.
d) DMA controller.

15. In I/O mode 2 Port C is used for

a) Simple I/O. b) Handshake. c) BSR mode. d) No effect.

16. USART stands for

a) Universal Asynchronous Receiver /Transmitter.
b) Universal Synchronous/Asynchronous Receiver /Transmitter.
c) Universal Asynchronous Receiver /Transmitter.
d) Universal Receiver /Transmitter.

17. 8086 is _____

a) 16 bit processor. b) 8 bit processor.
c) 32 bit processor. d) 64 bit processor.

18. AAA stands for

a) ASCII adjust for addition.
b) ASCII adjust for subtraction.
c) ASCII adjust for multiplication.
d) ASCII adjust for division.

19. The number of address lines required to address 64Kilo Byte memory is

a) 12 address lines. b) 20 address lines.
c) 10 address lines. d) 16 address lines.

20. If MN/$\overline{MX}$ pin is asserted low, then 8086 is operating in

a) Maximum Mode. b) Minimum mode.
c) Min/Max Mode. d) high/low mode.

PART B (5 x 16 = 80 Marks)

21 a) With neat block diagram explain the architecture of 8085A microprocessor.

(OR)

b) With suitable examples, explain the logical instructions of 8085.

22 a) List the addressing modes of 8085 explain each mode with examples.

(OR)

b) Write an assembly language program using 8085 instruction to convert ASCII code into binary code

23 a) Briefly explain the working of programmable interrupt controller.

(OR)

b) Briefly explain the working of DMA controller.

24 a) With a block diagram explain the working of programmable timer.

(OR)

b) Using 8255 PPI, write an assembly language program to generate a square wave in BSR mode.

25 a) Discuss the instruction set and various addressing modes of 8086 microprocessor.

(OR)

b) With neat block diagram explain the architecture of 8085A microprocessor

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