Register Number.....

B.E. / B. TECH. DEGREE EXAMINATIONS: APRIL/MAY 2009

Third Semester

U07CS305 DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to **B.E. Computer Science and Engineering** and **B. Tech. Information Technology** Branches)

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 x 1= 20 Marks)

1. x+x'=
   a. 0 b. 1 c. x d. x'
2. (x+y)(x+y')=
   a. x+y b. xy c. 0 d. 1
3. The algebric function for NAND gate is
   a. F=(x+y)' b. F=(x'+y') c. F=xy d. F=(xy)'
4. n variable can be combined to form _____ minterms
   a. 2n b. n+2 c. 2^n d. n
5. Fanout is
   a. Maximum Number of load that can be connected in the input
   b. Maximum Number of load that can be connected in the output
   c. Minimum Number of load that can be connected in the input
   d. Minimum Number of load that can be connected in the output
6. Scottky Transistor has
   a. A schottky diode between base and collector
   b. A schottky diode between collector and Emitter
   c. A schottky diode between base and emitter
   d. A schottky diode between base and emitter in reverse bias
7. Emitter coupled logic is
   a. non saturated digital logic family
   b. saturated digital logic family
   c. saturated register logic family
   d. non saturated diode logic family
8. Field effect transistor is a
   a. Uni-polar Transistor
   b. Bipolar transistor
   c. Tri-polar Transistor
   d. Uni-polar Diode
9. Half adder adds
   a. Carry bit b. 2bits c. 3 bits d. 2 bits + carry bit

10. Decoder is

a. N input to 2n output
b. N input to 2^n output
c. 2n input to 2n output
d. 2^n input to n output

11. High impedance state behaves like a

a. Open Circuit b. Closed Circuit c. Logical High d. Logical Low

12. The number of output from a 4 bit carry look ahead adder is

a. S1S2S3S4+C b. S1S2S3+C c. S1S2S3S4S5+C d. S1S2S3S4

13. Sequential Circuit is a combination of

a. Combination Circuit + Sequential Elements
b. Combination Circuit + memory Elements
c. Digital circuit + sequential Elements
d. Digital Circuit + Combination Elements

14. A flip flop can maintain its state

a. Indefinitely
b. For 5 seconds
c. For 10 Seconds
d. Will not maintain

15. Every Flip flop in a register can store up to

a. 8 bits b. 4 bits c. 2 bits d. 1 bit

16. A decimal counter follows a sequence of

a. 0 to A b. 0 to 9 c. 0 to 7 d. 0 & 1

17. CPLD is a

a. Complex Programmable Logic Device
b. Combination Programmable Logic Display
c. Complex Preventable Logic Display
d. Combined programmable Logic Device

18. Hamming code is used to

a. Detect the error
b. Correct the error
c. Detect and Correct the error
d. Correct any no of Errors

19. In SRAM Content will be available

a. Till the power goes
b. Till the refreshing is done
c. Even after the power goes
d. Even after the refreshing is not done

20. The type of RAM use in Computers are

a. SRAM b. DRAM c. KRAM d. PLD

PART B (5 x 16 = 80 Marks)

21. a. i, Express the Boolean function F=A+B'C in sum of min terms (8)

ii. Express the Boolean function F=xy+x'z in product of max terms (8)

(OR)

b. Discuss the Levels in NAND implementation with example (16)

22. a. Explain the special characteristics of digital integrated circuits (16)

(OR)

b. Discuss in detail about the complementary MOS circuits (16)

23. a i. Explain the concept of full adder (4)

ii. Draw and Explain 4 bit adder subtracter (12)

(OR)

b Draw and Explain quadruple 2 to 1 line multiplexer (16)

24. a. i Discuss the various latches with diagram (8)

ii Draw and Explain the edge triggered Master Slave D Flip-flop (8)

(OR)

b. Explain the concept of 4 bit binary counter with parallel load with diagram. (16)

25. a. Elucidate the write and read operation in RAM with the timing diagram(16)

(OR)

b. Explain in detail about the sequential programmable devices (16)

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