Register Number.....

B.E. DEGREE EXAMINATIONS: APRIL /MAY 2009

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U07EC305 Electronic Circuits I

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 × 1 = 20 Marks)

1. Transistor is in saturation when

   A. $I_B = I_C$, B. $I_B = IC / \beta_{dc}$, C. $I_B = O$, D. $I_B < I_C / \beta_{dc}$,

2. Biasing is required to

   A. decide the operating region,
   B. increase the input resistance
   C. increase the input resistance,
   D. supply the necessary power for desired amplification
   E. Answer (a) and (b)
   F. Answer (c) and (d)

3. Negative feedback exists in the

   A. fixed bias circuits, B. collector-to-base bias circuit,
   C. emitter bias circuit, D. Answer (a) and (b)
   E. Answer (b) and (c)

4. A JEET has I_{DSS} = 8mA and V_{GS} (off) = -4V. Than the source resistance is,

   A. 2Ω, B. 5 Ω, C. 500 Ω, D. 2K

5. In CB configuration the dependable current source has magnitude equal to

   A. $h_{fb} I_b$, B. $h_{fb} I_e$, C. h_{fe}, D. $h_{fc} I_e$

6. The Darlington connection

   A. increases input resistance, B. increases current gain
   C. decreases current gain, D. increases voltage gain
   E. Answer (a) and (b) F. Answer (a) and (d)

7. In a common source amplifier, V_{ds} = 4.2 V_{rms} and V_{gs} = 140 mV_{rms}. The voltage gain is

   A. 4.2, B. 42, C. 30, D.20.45

8. Common mode rejection ratio is

A. $CMRR = \dfrac{R_s + h_{ie} + 2R_E(1 + h_{fe})}{(R_s + h_{je})}$

B. $CMRR = \dfrac{R_s + h_{ie} + 2R_s(1 + h_{je})}{(R_E + h_{fe})}$

C. $CMRR = \dfrac{R_s + h_{fe} + 2R_s(1 + h_{je})}{(R_s + h_{ie})}$

D. $CMRR = \dfrac{R_E + h_{fe} + 2R_s(1 + h_{je})}{(R_E + h_{ie})}$

9. The bandwidth of an amplifier is determined by

A. the midrange gain, B. cut-off frequencies
C. the roll-off rate, D. the input capacitance

10. For a certain amplifier f_1 = 50 Hz and f_2 = 500 kHz then the bandwidth of amplifier is

A. 499.95 kz, B. 500.05 kHz, C. 500 kHz, D. 50Hz

11. The miller input capacitance of an amplifier is a function of

A. the input coupling capacitor, B. the voltage gain
C. the bypass capacitor

12. For high frequency analysis, the h-parameter model is not suitable because

A. It becomes complex at high frequency
B. H-parameter values are not constant at high frequencies
C. H-parameter values are not accurate at high frequencies
D. Answer (a) and (b)
E. Answer (a) and (c)

13. A silicon power transistor is operated with a heat sink with Θ_{SA} = 1.2 °C/W. The transistor is rated for 120 W at 25°C and has Θ jc=0.5°C/W. The mounting insulation has Θ cs = 0.65°C/W. What maximum power can be dissipated if the ambient temperature is 35 °C and $(Tj)_{max}$ = 200°C

A. 66.50 W, B. 68.75 W, C. 60.75 W D. 60.55 W

14. What is slope of the load line?

A. Positive of reciprocal of load resistance
B. Load resistance
C. Negative of reciprocal of load resistance
D. reciprocal of load resistance

15. The efficiency of class B is ----------than class A.

A. Lower, B. Higher, C. Same D. Very Low

16. Which transistor parameter is responsible for cross-over distortion?

A. Cut-in-voltage, B. Power, C. amplified D. Voltage

17. List the following parameters for half wave rectifier in terms of maximum current

A. I_{DC}, B. I_{RMS}, C. E_{DC}, D. Ripple factor

18. In a particular application single phase half wave rectifier using SCR is used. The average load voltage is 80V. if supply voltage is 230 V, 50Hz a.c., find the firing angle of the SCR.

A. $\alpha = 52.95°$, B. $\alpha = 56.95°$, C. $\alpha = 53.95°$ D. 54.65°

19. A step down switching regulator of 200 V. The switching frequency is 25 Hz while on period is 22 msec. Find the average voltage across the load

A. 120 V, B. 220 V, C. 110 V D. 210 V

20. Peak inverse voltage of diode is

A. 4 E_{sm}, B. 2 E_{sm}, C. 8 E_{sm} D. ½ E_{sm}

PART B (5 x 16 = 80 Marks)

21. (a) (i) Explain in detail the biasing of MOSFET. (8)

(ii) Prove that self bias is better bias compared to collector to base bias. (8)

(OR)

21 (b) (i) Prove that collector to base bias is better than fixed bias. (8)

(ii)Design a collector to base bias circuit to have operating point of (10 V, 4 mA). The circuit is supplied with 20 V and uses a silicon transistor of h_{fe} 250. (8)

22. (a) A common emitter amplifier with R_c = 5 k is driven by a voltage source of 1 KΩ internal resistor. Its output is connected to an emitter follower of R_e = 5 k across which output is connected to an emitter follower of R_e = 5 k across which output is taken. The hybrid parameters are;
h_{ie} = 2k = h_{ic} h_{oe} = 25μ siemen = h_{oc} $h_{re} = 6 \times 10^{-4}$ h_{fe} = 50
h_{fc} = -51 h_{re} = 1 Calculate the overall voltage gain at mid frequencies. (16)

(OR)

22. (b) Derive the expression for the voltage gain of

(i) Common source amplifier

(ii) Common drain amplifier configurations, under small signal low frequency conditions. (16)

23. (a) Derive the expression for CE short circuit current gain and current gain with resistive load, at high frequencies. (16)

(OR)

23 (b) (i) What is the effect of $C_{b'c}$ on the input circuit of a BJT amplifier at High frequencies? (12)

(ii) Define alpha out off frequency. (4)

24. (a) Prove that the maximum efficiency

(i) for class A transformer coupled power amplifiers is 50% and

(ii) for class B is 78.5% (16)

(OR)

24 (b) Draw a transformer coupled class B amplifier using PNP transistors and explain its operation, with the waveforms at various terminals. What is the modification done to alter it to function as a class AB amplifier? What is the need for such a modification? (16)

25. (a) Describe the working principle of full wave rectifier and derive the expression for the ripple factor, testifier efficiency V_{DC}, I_{RMS}, I_{DC} and V_{RMS}. (16)

(OR)

25.(b) Draw the block diagram of a switch mode power supply and explain the operation. (16)

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