Register Number.....

B.E. DEGREE EXAMINATIONS: APRIL/MAY 2009

Fourth Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

U07EI403 Digital Logic Circuits

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 x 1 = 20 Marks)

1. Logical expression Y=A+AB is equivalent to

   (a) Y=AB (b) Y=A (c) Y=1 (d) Y=A+B

2. Which of the following is a self complementing code?

   (a) 8421 code (b) Excess 3 code

   (c) Pure binary code (d) gray code

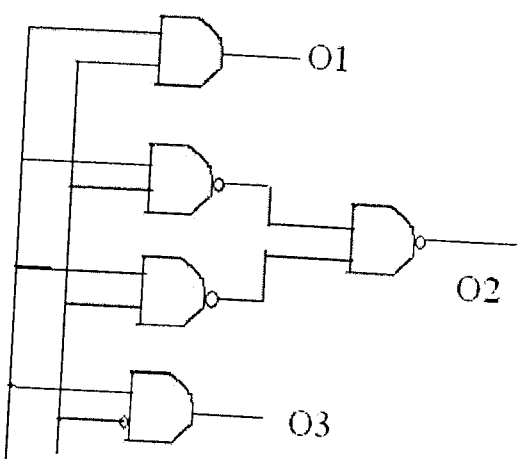
3. The binary fraction 0.0111 in decimal form is equal to

   (a) 0.4375 (b) 0.6225 (c) 0.8325 (d) 0.1105

4. The decimal is encoded as 1100 0101 in

   (a) 8421 code (b) 4421 code (c) 2421 code (d) 2221 code

5. The circuit shown in the figure is



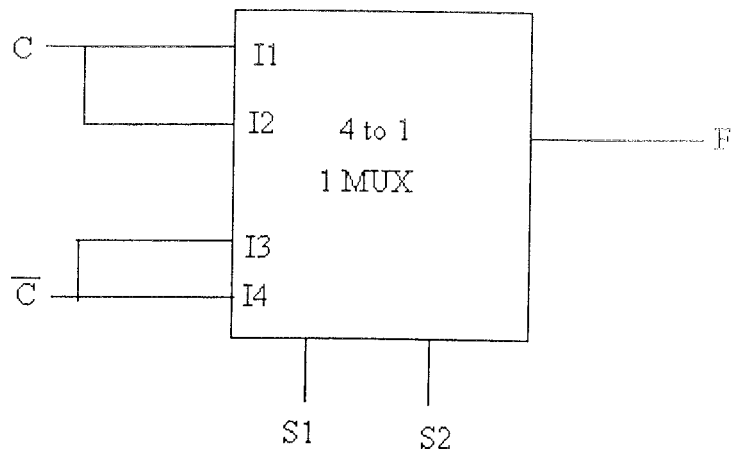
   (a) An adder

   (b) A subtractor

   (c) Parity Generator

   (d) Comparator

6. The logic realized by circuit shown in figure below is



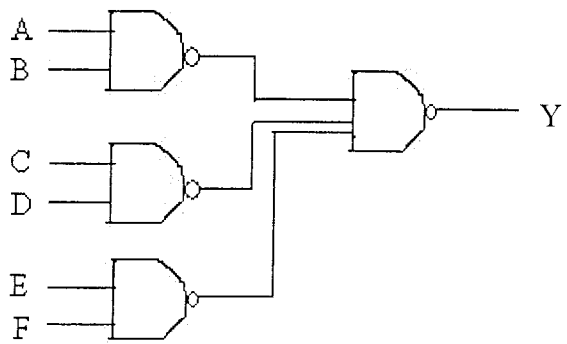
(a) F=A $\odot$C (b) F=A $\oplus$ C (c) F=B $\odot$ C (d) F= B+C

7. The output of a logic gate is '1' when all its inputs are at logic'0' The gate is either

(a) A NAND gate or an EX-OR gate (b) A NOR gate or an EX-NOR gate

(c)A OR or an EX-NOR gate (d) A AND or an EX-OR gate

8. The output of gated network in the figure is



(a) $Y=(AB)^{|}(CD)^{|}(EF)^{|}$ (b) $Y=(AB)^{|}+(CD)^{|}+(EF)^{|}$

(c) Y=AB+CD+EF (d) Y= (A+B)(C+D)(E+F)

9. A Mod-2 counter followed by a mod-5 counter is

(a) Same as a mod- 5counter followed by a mod-2 counter

(b) A decade counter

(c) A mode -7 counter

(d) A Mod 6 counter

10. The characteristics equation of the T-FF is given blow

(a) $Q^{+}=T\,'Q'+TQ$ (b) $Q^{+}=TQ'+QT'$ (c) $Q^{+}=TQ$ (d) $Q^{+}=TQ'$

11. A 4 bit binary ripple counter uses flip flops with a propagation delay time of each 25ns, The Maximum possible time required for change of state will be
(a) 25ns (b) 75ns (c) 50ns (d) 100ns

12. Which of following statement is incorrect?
(a) A flip-flop used to store 1bit information
(b) Race around condition occurs in JK flip flop when both the inputs are 1
(c) Master slave configuration is used in flip flops to store 2 bits of information
(d) A transparent latch consists of a D type flip flop

13. Which one of the following can be used to change data from special code to temporal code ?
(a) Shift registers (b) A/D converters (c) Counters (d) combinational circuits

14. The q output of JK flip flop is '1' the output does not change when a clock pulse is applied the inputs J and K will be respectively (x denotes don't care state)
(a) 0 and X (b) X and 0 (c) 1 and 0 (d) 0 and 1

15. A switch tail ring counter is made by using a single D FF the resulting circuit is
(a) SR flip flop (b) JK Flip flop (c) D Flip flop (d) T Flip flop

16. Design of a sequential circuit having nine state minimum number of memory elements required is
(a) 3 (b) 4 (c) 5 (d) 9

17. A SCHOTTKY dam pint is restored to in TTL gates
(a) To reduce propagation delay (b) To increase noise margins
(c)To increase packing density (d) To increase fanout

18. A PLA can be used
(a) As a Microprocessor (b) As a dynamic memory
(c)To realize a sequential logic (d) To realize a combinational of logic

19. Which of the following using the least power?
(a) TTL (b) CMOS (c) ECL (d) RTL

20. PROM are used to store
(a) Buck information (b)Sequential information
(c)Information to be accessed rarely (d) Relatively permanent information

PART B (5 x 16 = 80 Marks)

21. (a) Reduce the function using K-map technique.
(i) $F(A,B,C,D,E) = \sum m(1,4,8,10,11,20,22,24,25,26) + d(0,12,16,17)$ (8)
(ii) $F(A,B,C,D) = \prod M(1,2,4,5,7,8,10,11,13,14)$ (8)

(OR)

(b) Using Tabulation method simplify the Boolean expression (16)
$F(D,C,B,A) = \sum (0,5,7,8,9,10,11,14,15)$

22. (a) Design a BCD to Excess 3 code Converter (16)

(OR)

(b) (i) Implement the function F(A,B,C,D)= A' BD' + ACD + B 'CD + A ' C 'D using 8 to 1 multiplexer and 4 to 1 multiplexer (12)

(ii) Design the full subtractor . (4)

23.(a) Construct the Transistion table ,State table and State Diagram for the moore Sequential circuit expression given below (16)

$F=A \oplus B.$

$J_A=B$ $K_A=X\,B$

$J_B=X$ $K_B=X \oplus A.$

(OR)

(b) (i) Design a 3 bit binary counter using T flip flop (8)

(ii) Design a 4 bit Johnson counter and explain its operation (8)

24. (a) Explain the various steps in the analysis of asynchronous sequential circuits with suitable example. (16)

(OR)

(b)Design asynchronous Sequential circuit is describe by the following excitation and output function $Y = X_1 X_2 + (X1 + X_2) Y$. (16)

(i) Draw the logic diagram.

(ii) Derive the transition table and output map.

(iii) Describe the behavior of the circuit.

25. (a) Implement the given function using PAL and PLA. (16)

(i) $F1 = \sum m (1,2,4,6)$

(ii) $F2 = \sum m (0,1,6,7)$

(iii) $F3 = \sum m (2,6)$

(OR)

(b) (i) Draw the circuit diagram of a TTL two input NAND gate with totem pole output and explain its operation. (10)

(ii) Draw the circuit diagram of CMOS inverter and NAND gate. (6)

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