Register Number.....

B.E. DEGREE EXAMINATIONS: APRIL / MAY 2009

Third Semester

MECHATRONICS ENGINEERING

U07MH303 Digital Electronics

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 x 1 = 20 Marks)

1. $\left(\overline{A+B}\right)$ is equal to

   a. $\overline{A}+\overline{B}$ b. $\overline{A}.\overline{B}$ c. $A+\overline{B}$ d. $\overline{A.B}$

2. Reduce the expression $A+\overline{A}B$

   a. $A+B$. b. AB c. A-B. d. $A \oplus B$

3. The addition of 1001 and 0101 results in

   a. 1010 b. 1100 c. 1110 d. 1111

4. Use De Morgans Theorem to find Complement of $A+BC$

   a. $\overline{A}.\left(\overline{B}+\overline{C}\right)$ b. $\left(\overline{A}+B\right)(C)$ c. $A+B+C$ d. $\overline{A+BC}$

5. The gate which is called as Universal gate is

   a. NAND. b. AND. c. OR d. EX-OR

6. A Combinational Circuit that performs the addition of three bits is called as

   a. Half Adder b. Full Adder. c. Half subtractor d. Full subtractor.

7. A Multiplexer is

   a. Many i/p, single o/p b. Many i/p c. Single o/p d. Single i/p, many o/p

8. An Encoder is a

   a. Combinational circuit b. Sequential circuit
   c. Synchronous circuit d. Asynchronous circuit

9. How many ADDRESS location are made for a 16 bit Address

   a. 2^{16}. b. 2^{61} c. 2^{12} d. 2^{6}

10. Register is a

    a. Temporary storage device. b. Permanent storage device memory.
    c. Memory. d. ROM At both the ends.

11. Fundamental Mode circuit depends,

    a. only one input variable change at a time b. On the pulses of input variable.
    c. Width of pulses. d. Only on pulses not on levels.

12. Unclocked flip-flops are called as
a. Latches b. Flip-flops c. Clock d. Modes.

13. The memory elements in synchronous sequential circuit are
a. Clocked Flip Flop. b. Unclocked Flip-flop.
c. Latches. d. Flip-flops.

14. Races can be avoided by making proper binary assignment to the
a. State variables. b. Total State c. Internal State d. Delay.

15. Flow tables depends on
a. Letter symbols. b. Binary values c. Critical race. d. Non-critical race.

16. Primitive Flow table has only
a. 1 stable state. b. 2 stable state. c. 4 stable state d. 3 stable state.

17. The acronym PLA stands for
a. Process Logic Array. b. Programmable Logic Array.
c. Process Large Array. d. Programmable Large Array.

18. A condition state in ASM chart is denoted by the symbol,
a. Rectangle. b. Circle. c. Rhombus d. Square.

19. When a circuit goes through a unique sequence of unstable states it is said to have
a. Cycle. b. Flow table c. Transition state. d. Race.

20. T Flip Flop has
a. 1 Input. b. 2 Input c. 3 Input d. 4 Input.

PART B (5 x 16 = 80 Marks)

21. (a) (i). Show that.

1. $\left(\overline{\overline{A}B + A\overline{B}}\right) = \overline{A}B + A\overline{B}$ (4)

2. $\left(\overline{\overline{A}B + A\overline{B}}\right) + \overline{A}.\overline{B} + AB$ (4)

(ii) Reduce the Boolean Expression.

1. $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$ (4)

2. $AB + \overline{A}C + BC$ (4)

(OR)

(b) Simplify the Expression by Tabulation Method (16)

$$F(A,B,C,D) = \sum (1,4,6,7,8,9,10,11,15)$$

22. (a) Design a BCD to Seven Segment Code Converter. (16)

(OR)

(b) Explain the working of J-K Master Slave Flip Flop and T Flip flop and draw the truth table. (16)

23. (a) Explain the Working of Ring Counter and Johnson's counter. (16)

(OR)

(b) (i) Explain the Working of 4 bit Shift Right Register (8)

(ii) Design and Explain the Working of Parallel to Serial conversion. (8)

24. (a) An asynchronous sequential circuit is described by the following excitation and output function. (16)

$$Y = X_1\overline{X}_2 + \left(X_1 + \overline{X}_2\right)Y \;\; ; \;\; Z = Y$$

(i) Draw the logic diagram of the circuit.

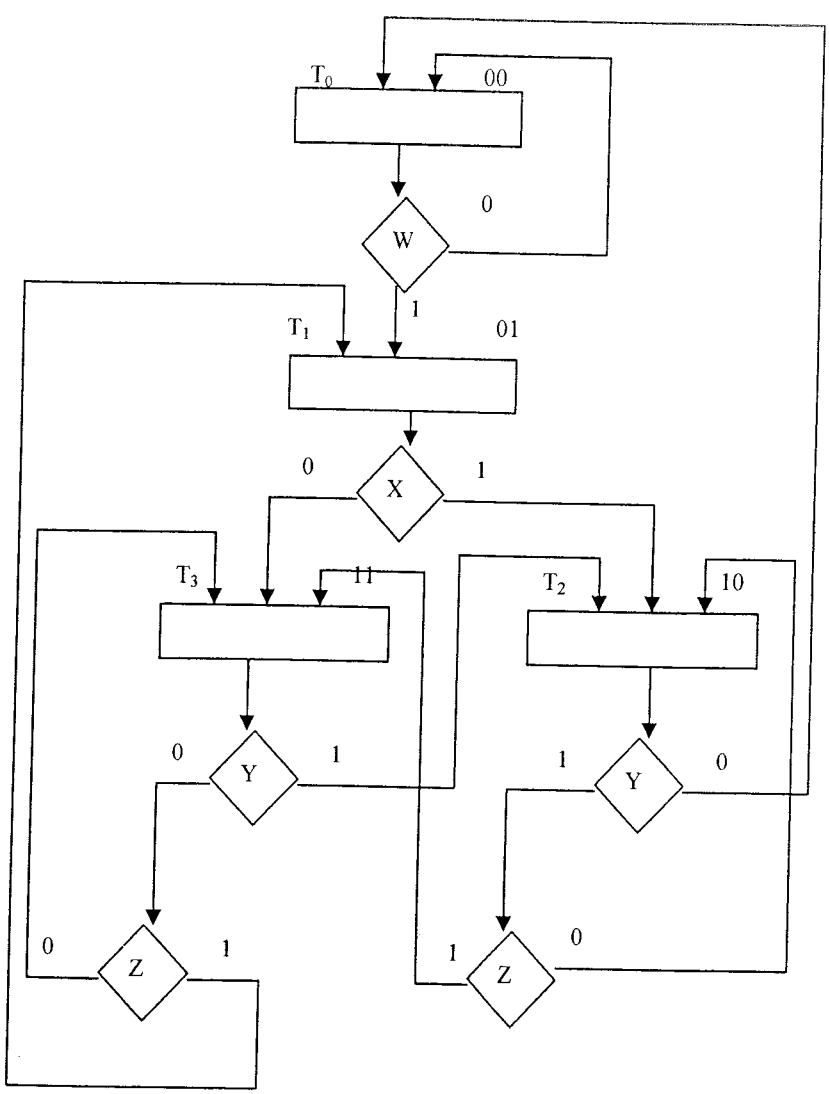
(ii) Derive the transition table and output map.

(OR)

(b) An asynchronous sequential circuit has two internal states and one output. Excitation and output function describing the circuit are as follows: - (16)

$$Y_1 = X_1X_2 + X_1Y_2 + X_2Y_1$$
$$Y_2 = X_2 + X_1Y_1Y_2 + X_1Y_1$$
$$Z = X_2 + Y_1$$

25. (a) Design Multiplexer from the below ASM chart. (16)



Or

(OR)

(b) Draw an ASM Chart and state diagram for the Synchronous circuit having the following description: (16)

The circuit has control input C, clock and outputs X, Y, Z.

1. If C=1, on every rising edge of the clock code on output x, y and z changes from 000→010→100→110→000 and repeats

2. If C=0, the circuit holds the present state.

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