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B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2008.

Fourth Semester

Information Technology

CS 1304 — MICROPROCESSORS AND MICROCONTROLLERS

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the number of machine cycles and T-states requires to complete the execution of the 8085 instruction MOV M,A.

2. Let PC = 8500 H and SP = E000 H when a current instruction is being executed by 8085. What will be new value of these registers, when a device interrupts the processor on RST 5.5?

3. What are the maximum address space and data bus width of 8086 processor?

4. Mention the addressing modes of the following 8086 instructions: mov al, disp[bx]; mov ah, disp[bx][si].

5. The CS contains A820, while the IP contains CE 24. What is the resulting physical address?

6. What does it imply if the states of 8086 signals –BHE and A 0 are at 0 and 1, respectively?

7. A file of size 100 KB is being sent on a serial link with the following communication parameters: 9600 bps, 2 stop bits, even parity and 8 bits/char. Calculate the best case transmission time.

8. What does it imply if 8259's ICW 1 bit fields LTIM and SNGL bits are set to zero?

9. What is the possible branching range when an AJMP/ACALL of 8051 instruction is executed?

10. Name the interrupt sources of 8051 for which the priority levels are highest and lowest, respectively.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the functions of the following signals of 8085: RST 7.5, TRAP, HOLD, and -INTA. (8)

(ii) Draw and explain the use of bits in PSW in 8085. What are the flags affected by the MVI M,00 and XRA A instructions? (8)

Or

(b) (i) Enumerate the addressing modes of 8085 instruction set with suitable examples for each. (8)

(ii) Write an assembly language program using 8085 instruction mnemonics that converts a given 2 digit BCD into its equivalent hexadecimal value. Make the program self explanatory with appropriate comments. (8)

12. (a) (i) List and explain the use of segment registers in 8086. (8)

(ii) Explain how instruction pipeline works in 8086 and mention how it helps in improving CPU's performance. (8)

Or

(b) (i) Explain the physical memory organization in an 8086 system. (8)

(ii) Distinguish between the following pairs: NEAR and FAR procedures, macros and subroutines. (8)

13. (a) (i) Explain how address signals are de-multiplexed from 8086 Address/Data bus using a schematic diagram and an appropriate timing diagram. (8)

(ii) What happens when 8086 is operated in Maximum mode? List the signals that are unique in this mode. (8)

Or

(b) (i) List and explain the use of index and pointer registers in 8086. (8)

(ii) Explain the basic bus access control and arbitration schemes used in multiprocessor systems. (8)

14. (a) (i) Interface four 8K chips of RAM and two 8K chips of EPROM with 8086. Interface the RAM bank at a segment address 0 B 00 H and the EPROM bank a physical address F 8000 H. (8)

(ii) Illustrate the working of Mode 3 operation of 8253 timer with a suitable timing diagram. (8)

Or

(b) (i) Explain the functioning of scanned keyboard mode with 2-key lockout and N-key roller of 8279. (8)

(ii) Differentiate between synchronous and asynchronous modes of serial communications. Interpret the mode of operation of 8251 if its mode instruction command word is initialized to 0 FEH. (8)

15. (a) (i) Draw and explain the functions of bits in TMOD and TCON registers of 8051. (10)

(ii) Explain how 8051 distinguishes between internal and external ROMs. (6)

Or

(b) (i) Write a brief note on interrupts and their priorities of 8051. Draw the format and explain the bit functions of interrupt enable register. (10)

(ii) List the addressing modes of 8051 and give a specific example for each of them. (6)
