Reg. No. : | | | | | | | | | | | |

A 1213

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2008.

Third Semester

Mechatronics Engineering

EC 154 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(21 \cdot 2)_{10}$ into a binary number.

2. Write down the truth table of universal gates.

3. Simplify $A + AB$.

4. What is a PLA?

5. How many flip flops are necessary to realise a decade counter?

6. Draw the internal circuit of a SR flip flop.

7. Define a cycle.

8. What is a dynamic hazard?

9. What is an ASM chart?

10. What is an asynchronous sequential circuit?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Find out the following :

(1) $(F5 \cdot 3B)_{16} = (\quad)_8$

(2) $(217)_8 = (\quad)_2$ (3)

(ii) Add $(-176)_{10}$ and $(-204)_{10}$ using 2s complementation. (5)

(iii) Simplify the following using K-map

$$f = \Sigma m(1,2,5,10,11,12) + \Sigma d(3,6,9)$$

Implement the simplified function using NAND gates only. (8)

Or

(b) (i) Find the 2s complement equivalent of $(-119)_{10}$ and $(95)_{10}$. (3)

(ii) Create the truth table and the logic equations for a circuit which controls a light (L) through two switches (A and B). The light is to be on (TRUE) when both A and B are TRUE and either switch can independently turn the light off and on. (5)

(iii) Prove or disprove the following identity. If it is proven, does it follow that $ACD = 0$?

$A'C + CD + AB'C' = A'C + CD + AB'C' + ACD$. (8)

12. (a) Design the following circuits.

(i) Full adder and Half subtractor. (8)

(ii) 4 to 1 multiplexer and 2 × 4 Demultiplexer. (8)

Or

(b) (i) Design a binary to Gray code converter. (10)

(ii) Write notes on PAL and PLA. (6)

13. (a) (i) Design a mod-12 counter. Explain its working with a timing diagram. (10)

(ii) Convert a SR flip flop into a D flip flop. Explain its working. (6)

Or

(b) (i) Explain the working of a master-slave JK flip-flop.

(ii) Explain the working of a RAM cell.

(a) Design an asynchronous circuit that will output only the first pulse received whenever a control input is asserted from LOW to HIGH state. Any further pulses should be ignored.

Or

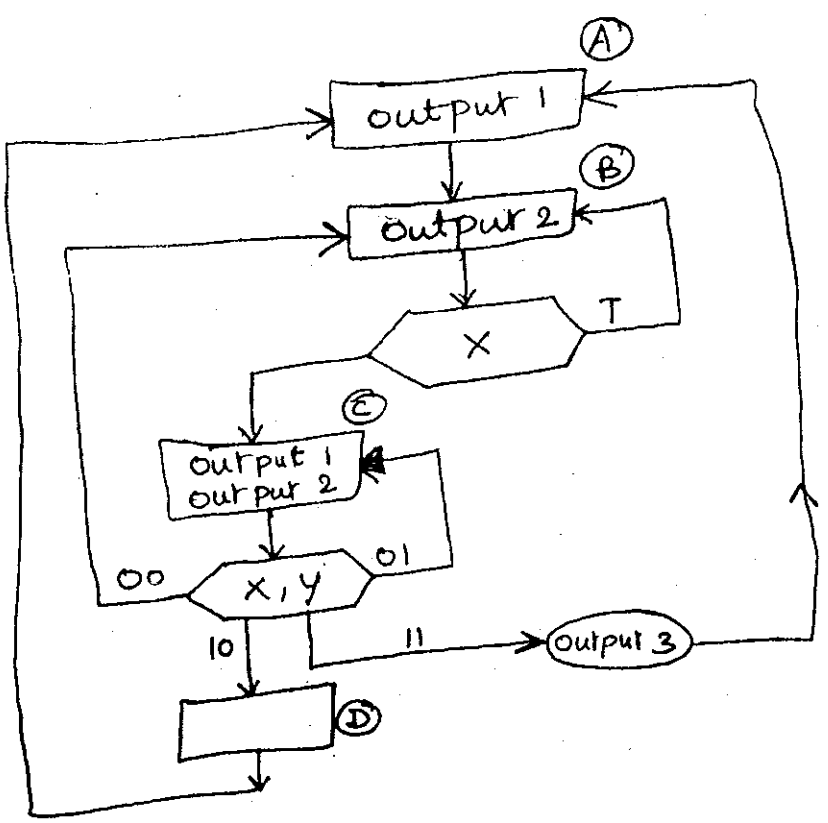
(b) (i) What is a race condition? Explain the types of races with example. (6)

(ii) Obtain a static hazard free asynchronous circuit for the following switching function (8)

$$f = \Sigma(0,2,4,5,8,10,14)$$

(iii) Distinguish between completely and incompletely specified state machines. (2)

15. (a) Using the ASM chart shown below, draw the state transition table for a one-hot controller and write the design equations.



Or

(b) Using the ASM chart shown below, draw a state transition table and produce a set of design equations for a minimal flip-flop realisation.