Reg. No. : | | | | | | | | | | | |

B 2153

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2008.

Fourth Semester

Electronics and Communication Engineering

EC 242 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL the questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert the following numbers to decimal :

   (a) $(1001001 \cdot 011)_2$

   (b) $(0.342)_6$.

2. Express the following functions in a sum of minterms and a product of maxterms.

   (a) $F(x,y,z) = (xy + z)(y + xz)$

   (b) $F(w, x, y, z) = y'z + wxy' + wxz' + w'x'z$.

3. Calculate the noise margin of ECL gate.

4. Draw the interconnection of I^2L gates to form a 2×4 decoder.

5. A combinational circuit has four input and one output. The output is equal to 1 when (a) all the inputs are equal to 1 or (b) none of the inputs are equal to 1 or (c) an odd number of inputs are equal to 1. Obtain the truth table.

6. How many don't care inputs are there in BCD adder?

7. Show the logic diagram of a clocked RS flip-flop with four NAND gates.

8. What is the difference between serial and parallel transfer? What type of register is used in each case?

9. Verify that Fig. 1 is free of critical race :

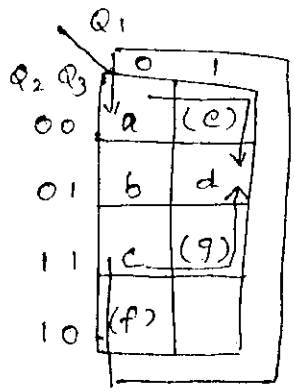

Fig. 1.

10. How can essential hazards be eliminated from a network?

PART B — ($5 \times 16 = 80$ marks)

11. (a) Given two Boolean functions F_1 and F_2 :

(i) Show that the Boolean function $E = F_1 + F_2$ obtained by ORing the two functions, contains the sum of all the minterms in F_1 and F_2. (8)

(ii) Show that the Boolean function $G = F_1 F_2$ obtained by ANDing the two functions. Contains those minterms common to both F_1 and F_2. (8)

Or

(b) (i) With the use of maps, find the simplest form in sum of product of the function $F = f\,g$, where f and g are given by

$$f = wxy' + y'z + w'yz' + x'yz'$$

$$g = (w + x + y' + z')(x' + y' + z)(w' + y + z').$$

(ii) Simplify the boolean function F using don't care condition d in (1) sum of production and (2) product of sum ; using tabulation method.

(A) $F = ACE + A'CD'E' + A'C'DE$

$d = DE' + A'D'E + AD'E'$ (4)

(B) $F = B'DE + A'BE + B'C'E + A'BC'D'$

$d = BDE' + CD'E'$. (4)

12. (a) (i) (1) Determine the highlevel output voltage of RTL gate for a fan-out of 5.

(2) Determine the minimum input voltage required to drive an RTL transistor to saturation when h_{FE} = 20.

(3) From the results in (1) and (2) determine the noise margin of the RTL gate when the input is high and fan out is 5. (8)

(ii) With neat circuit diagram explain the analysis characteristics of TTL logic gate. (8)

Or

(b) (i) The MOS transistor is bilateral, is current may flow from source to drain or from drain to source. Using this property, derive a circuit that implement the Boolean function.

$$Y = (AB + CD + AED + CED)'$$

using six MOS transistors. (8)

(ii) Show the circuit of CMOS transistors using

(1) four-input NAND gate (4)

(2) four-input NOR gate. (4)

13. (a) (i) Design a combinational circuit to check for even parity of four bit. A logic-1 output is required when four bits do not constitute an even parity. (8)

(ii) Design a combinational circuit that detect an error in the representation of a decimal digit in BCD. (8)

Or

(b) (i) A combinational circuit is defined by the following three functions :

$$F_1 = x'y' + xyz'$$

$$F_2 = x' + y$$

$$F_3 = xy + x'y'$$

Design the circuit with decoder and external gates. (8)

(ii) Derive the PLA program table for a combinational circuit that squares a 3-bit number. Minimize the number of product terms. (8)

14. (a) Design the circuit of 4-bit register that converts the binary number stored in the register to its 2's complement value when input x =1. The flip-flops of the register are of RST type. This flip-flop has three inputs, two inputs have RS capabilities and one has a T capability. The RS inputs are used to transfer the 4-bit number when an input y = 1. Use the T-input for the conversion. (16)

Or

(b) (i) Design a synchronous BCD counter with J-K flip-flop. (8)

(ii) Briefly explain Magnetic-core memory. (8)

15. (a) (i) Using the following assignment fig. 2 find the expanded flow table. Note that although, a direct transition from a_1 to d_1 or d_2 is not possible a transition from a_1 to a_2 to d_2 is possible since a_1 and a_2 are equivalent states. (8)

a_1	a_2
b_1	b_2
c_1	d_1
c_2	d_2

Fig. 2

(ii) A sequential network has two input (X_1, X_2) and one output (Z). If the input sequence 00, 01, 11 occurs, Z becomes 1 and remains 1 until the input sequence 11, 01, 00 occurs. In this case Z becomes 0 and remains 0 units the first sequence occurs again. Make proper assignment for this and realize the flow table with S-R flipflop and gates. (8)

Or

(b) (i) Find all of the essential hazards in the following flow table. For each hazard, specify the initial value of $X_1X_2Q_1Q_2$ and which input variable is changing. How can essential hazard which occurs starting in b be eliminated? (8)

			X_1X_2			
	Q_1	Q_2	00	01	11	10
a	0	0	(a)	b	(a)	d
b	0	1	a	(b)	c	–
c	1	1	–	d	(c)	d
d	1	0	a	(d)	a	(d)

(ii) Find a hazard-free realization for each of the following functions using only 3-input NOR gates :

(1) $f(a,b,c,d) = \sum m\ (0, 2, 6, 7, 8, 10, 13)$ (4)

(2) $f(a,b,c,d) = \sum m\ (2, 3, 6, 7, 8, 10, 13)$ (4)