Reg. No. : | | | | | | | | | | | |

# C 3234

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2008.

Third Semester

(Regulation 2004)

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Common to B.E (Part Time) Second Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(367)_{10}$ into Excess – 3 code.

2. Express Gray code 10111 into binary numbers.

3. Write the Boolean function of an XOR gate give its truth – table.

4. List the advantages of PLD's. (Programmable Logic Devices)

5. Convert a T-FF into an S-R FF. Draw the circuit.

6. Draw the state diagram of a MOD-10 counter.

7. Explain Dynamic Hazard.

8. What is meant by Race?

9. Explain 'write operation' with an example.

10. Draw the block diagram of Dynamic RAM cell.

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Obtain the canonical POS for

$F(A,B,C) = (A + B')(B + C)(A + C')$ (6)

(ii) Using k-map method obtain the minimal SOP and POS expressions for the function.

$F(x,y,z,w) = \sum(1,3,4,5,6,7,9,12,13)$. (10)

Or

(b) (i) Explain weighted BCD+2421 codes. (10)

(ii) Apply Demorgan theorem for the function $\overline{(A + B + C)D}$. (3)

(iii) Find the complement of A+BC+AB. (3)

12. (a) (i) Implement the function with a multiplexer.

$F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$. (6)

(ii) Draw and explain the working of a carry-look ahead adder. (10)

Or

(b) (i) Explain the operation of a 4 bit magnitude comparator circuit. (10)

(ii) Explain even parity checker. (6)

13. (a) (i) Design a sequential circuit with JK flip flop to satisfy the following state equations

$A(t+1) = A'B'C\,D + A'B'C + ACD + AC'D'$

$B(t+1) = A'C + CD' + A'BC'$

$C(t+1) = B$

$D(t+1) = D'$. (10)

(ii) Draw the logic diagram of a D-FF using NAND gates and explain. (6)

Or

(b) (i) With a neat circuit explain a universal shift register. (12)

(ii) Differentiate a Moore machine and a Mealey machine. Give the block diagram. (4)

14. (a) What is a Hazard? Explain the different types of Hazards. What is an essential Hazard? Discuss in detail how Hazards can be eliminated. (16)

Or

(b) Design a T-FF giving the flow table, state table, state assignment, excitation table and excitation map. (16)

15. (a) Explain :

(i) Memory decoding. (6)

(ii) Explain the various ROM. Organisations and give the uses for each type. (10)

Or

(b) (i) A combinational circuit is defined by functions.

$F_1(A,B,C) = \Sigma(3,5,6,7)$

$F_2(A,B,C) = \Sigma(0,2,4,7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs. (10)

(ii) Write notes on FPGA's. (6)

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