Reg. No. : | | | | | | | | | | | |

D 4158

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2008.

Fourth Semester

Electronics and Instrumentation Engineering

EC 1312 — DIGITAL LOGIC CIRCUITS

(Common to Instrumentation and Control Engineering)

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert $(26.24)_8$ to Hexadecimal format.

2. What is the largest binary number that can be expressed with 12 bits? What is the equivalent decimal and hexadecimal?

3. Simplify the following Boolean expressions to a minimum number of literals :

   (a) $\overline{x}yz + xz$

   (b) $ABC + \overline{A}B + AB\overline{C}$.

4. Obtain the truth table of the function

   $f = xy + x\overline{y} + \overline{y}z$.

5. Draw the logic diagram for D Latch.

6. Show that the characteristic equation for the complement output of JK flip flop is $Q'(t+1) = J'Q' + KQ$.

7. Define the purpose of Flow Table.

8. What do you mean by Race Conditions in Asynchronous Sequential Logic?

9. What are the important CMOS characteristics?

10. Draw the CMOS Logic Circuit for Inverter.

PART B — (5 × 16 = 80 marks)

11. (a) Perform the following conversion : (4 × 4 = 16)

(i) $(10110001\ 101011.111\ 100000110)_2$ to octal

(ii) $(0.513)_{10}$ to octal

(iii) $(0.6875)_{10}$ to binary

(iv) $(10110001101011.11110010)_2$ to hexadecimal.

Or

(b) (i) Simplify the Boolean function : (10)
$F(w, x, y, z) = \Sigma\ (1, 3, 7, 11, 15)$ which has the don't care conditions
$d\ (w, x, y, z) = \Sigma(0, 2, 5)$

(ii) Implement $F = A(CD + B) + B\overline{C}$ using NAND gates. (6)

12. (a) (i) Design the circuit for Full Adder. (8)

(ii) Draw the block diagram for a BCD Adder. (8)

Or

(b) (i) Construct 4 × 16 Decoder using Two 3 × 8 Decoders. (8)

(ii) Explain Priority Encoder with an example. (8)

13. (a) Implement the following boolean function using a multiplexer
$F\ (A, B, C, D) = \Sigma\ (1, 3, 4, 11, 12, 13, 14, 15)$.

Or

(b) Illustrate the Analysis with JK flip flop with state table and state diagram.

14. (a) (i) Design a 3 bit Binary Counter using T flip flop. (10)

(ii) Explain the procedure for designing synchronous sequential circuits. (6)

Or

(b) Illustrate analysis procedure of asynchronous sequential circuit with maps, transition table and flow table.

15. (a) Illustrate Asynchronous design with primitive flow table and transition table.

Or

(b) (i) Write about the principles of EPROM and FPGA. (8)

(ii) Compare the characteristics of TTL and ECL. (8)
