

B.E./B.TECH. DEGREE EXAMINATIONS: OCTOBER/NOVEMBER – 2008

Third Semester

U07CS305: DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to B.E. Computer Science and Engineering & B. Tech Information Technology Branches)

Time: Three Hours

Maximum Marks: 100

Answer ALL Questions:-

Part A(20 X 1 = 20 Marks)

- The hexadecimal equivalent of the binary number 11101101111010 is
a) EDEB b) 35572 c) FB7A d) 3B7A
- Two's complement representation of -8 is
a) 0111 b) 1000 c) 01000 d) 10100
- When representing in the following code, the consecutive decimal numbers differ only in one bit.
a) Excess-3 b) Gray c)BCD d) Hexadecimal
- The logic expression $AB + \overline{A}B$ can be implemented by giving inputs A and B to a two-input
a) NOR gate b) XNOR gate c)XOR gate d)NAND gate
- Propagation delay is measured in
a) milliseconds b)microseconds c)nanoseconds d)picoseconds
- FET is _____ transistor.
a) Bipolar b) Unipolar c) Tripolar d) Tetrapolar
- When a CMOS logic circuit is in a static state, its power dissipation is very
a) low b)high c) Moderate d)Normal
- The logic family which has the lowest propagation delay is
a)RTL b)DTL c)TTL d)ECL
- A full adder is a combinational circuit that forms the arithmetic sum of _____ bits
a) 5 b)4 c)8 d)3
- An encoder has
a) 2^n input lines and n output lines b) n input lines and 2^n output lines
c) 2^{n-1} input lines and n-1 output lines d) n input lines and 2^{n-1} output lines
- A 4-bit comparator is used to compare
a) two 8-bit binary words b) two 4-bit binary words
c) two 2-bit binary words d) two 6-bit binary words
- _____ is also called as a data selector.
a) Decoder b)encoder c)Multiplexer d)Demultiplexer
- _____ is a sequential circuit.
a) Parallel adder b)Serial adder c)Full adder d)Half adder
- Asynchronous counters are commonly called as
a)Johnson counter b)Modulo-n counter c) Ripple counter d)Shift counter
- If the register has both shifts and parallel load capabilities, then it is referred to as
a) unidirectional shift register b)bi-directional shift register
c) universal shift register d) parallel shift register
- The characteristic equation for D flip-flop is _____.
a) $Q_{n+1}=D$ b) $Q_{n+1}=D + 1$ c) $Q_{n+1}= JQ'+K'Q$ d) $Q_{n+1}= TQ'+T'Q$
- Read Only Memory is _____
a) static b) Dynamic c)non-volatile d)volatile
- The number of address lines in 64K x 10 memory will be
a) 8 b)16 c)32 d)64

