Register Number.....

B.E. DEGREE EXAMINATIONS: OCTOBER / NOVEMBER - 2008

Third Semester

MECHATRONICS ENGINEERING

U07MH 303 – Digital Electronics

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (20 x 1 = 20 Marks)

1. Hexa decimal addition of 2 B and 84 gives
   (a) AB (b) CF (c)AF (d) DE
2. Two's complement of $(10110)_2$ is
   (a) 10101 (b) 01010 (c) 11011 (d) 10111
3. Which of the following is proved in De Morgan's Theorem
   (a) A + A = 1 (b) $\overline{(A+B)} = \overline{A}.\overline{B}$ (c) A+B = A.B (d) A .1 = A
4. Find the standard POS expression
   (a) $(B+C)(A+\overline{B}) +(\overline{AC})$
   (b) $(A+B+C)+(A+\overline{B})(C+\overline{A})$
   (c) $(ABC)+(\overline{ACB})+(\overline{A}\,\overline{B}\,C)$
   (d) $(A+B)\,(\overline{A}+B)\,(A+\overline{B})$
5. Excess – 3 code for 1100 is
   (a) 0011 (b)1111 (c)invalid (d)1001
6. Combinational circuits are driven by clock pulses
   (a) True (b) False
   (c) Depends on the application (d) Independent of the Application
7. For the data bits 011 to be odd parity, the parity bit should be
   (a) 1 (b) 0 (c) don't care (d) 11
8. In which of the following logics, both "AND" and "OR" array are programmable
   (a) PLA (b) PAL (c) PLD (d) FPGA
9. Ripple counters are
   (a) Synchronous Counter (b) Asynchronous counter (c) Flip-Flop (d) Latches
10. In which of the following type, the input data bit are retrieved out with just one clock pulse.
    (a) SISO (b) SIPO (c) PISO (d)PIPO
11. In Which of the Flip-flop , invalid condition occurs for input's 1 & 1
    (a) JK (b) SR (c) both (d) AB
12. Master Slave flip-flop is
    (a) Edge triggered (b) level triggered (c) Forbidden (d) Two Bits Storage
13. Primitive flow table has
    (a) One stable state per row (b) 2 stable states per row
    (c) 3 stable states per row (d) 4 stable states per row

14. Race free assignments are used to avoid
    (a) Critical races (b) Non – Critical races
    (c) Latches (d) Forbidden Problem

15. Fundamental mode sequential circuits are
    (a) Pulse triggered (b) edge triggered (c) level triggered (d) No Trigger

16. Change of the output more than once as a result of single input variable change causes
    (a) Static hazard (b) Dynamic hazard
    (c) Essential hazard (d) Non Dynamic Hazard

17. ASM block of Moore circuit model is represented with conditional output symbols
    (a) True (b) False (c) Time Dependent (d) Time Independent

18. State Box in ASM Chart is
    (a) Time Dependent (b) Time Independent
    (c) Voltage Dependent (d) Voltage Independent

19. The Sum of all bit charges for all possible State transition is known as
    (a) Map (b) State Locus (c) Transition Table (d) Excitation Table

20. The other name of Controlled architecture is
    (a) Mclay Machine (b) Moore Machine
    (c) Data Processor (d) Synchronous Block

PART – B (5 X 16 = 80 Marks)

21. (a) (i) Convert the following (8)

    1. $(30.5)_{10}$ = ( )$_2$
    2. $(12.2)_8$ = ( )$_2$
    3. $(111101.111)_2$ = ( )$_{10}$
    4. $(306.D)_{16}$ = ( )$_2$

    (ii) Reduce the Boolean expression (8)

    1. ABC + ABC + C
    2. XY + XZ + XY
    3. 1 + ABC + AB
    4. X + XY + YZ

(OR)

(b) Simplify the expression by tabulation method. (16)

$F(A,B,C,D) = \sum (2,6,8,9,10,9,14,15)$

22. (a) (i) What is decoder and construct the 3 to 8 line decoder (8)

    (ii) Explain the operation of PAL (8)

(OR)

(b) (i) Design 4 x 1 Multiplexer circuit and write the truth table. (8)

    (ii) What is magnitude comparator and design 4 bit magnitude comparator. (8)

23. (a) (i) Construct 'D' flip flop from JK flip flop (8)

(ii) Design serial to parallel shift registers (8)

(OR)

(b)Construct 4 bit ripple counter and also design up/down synchronous counter (16)

24. (a) Define Hazards and discuss the Hazards in combinational and sequential circuit and how it is eliminated. (16)

(OR)

(b) Derive the primitive flow table when the condition start with the input condition JC = 11 and assign to it state 'a'. The circuit goes to state 'b' and the output Q Complements from 0 to 1 when 'c' changes from 1 to 0while T remains a '1'. Another change in the output occurs when the circuit goes from state 'c' to state 'd'. In this case, T = 1, 'c' changes from 1 to 0, and the output Q complements from 1 to 0.The other four states in the table do not change the output, because T is equal to 0. If Q us initially 0, it stays at 0, and if initially at 1, it stays at 1 even though the clock input changes.

25. (a) (i) What is ASM Chart explain each box in it. (8)

(ii) What is ASM Block? (8)

(OR)

(b) Explain ASM realization using Multiplexer (16)

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