Reg. No. : | | | | | | | | | | | |

C 3192

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2008.

Seventh Semester

Electrical and Electronics Engineering

CS 1034 — COMPUTER ARCHITECTURE

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulation 2004)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is an effective address?

2. What is the difference between direct and indirect address instruction?

3. Distinguish between hardwired and micro programmed control unit.

4. A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?

5. Why should the sign of remainder after a division be same as the sign of the dividend?

6. How many number of clock cycles that it takes to process 200 tasks in a six segment pipeline?

7. Why does DMA have priority over the CPU when both request a memory transfer?

8. What is the disadvantage of strobe method of data transfer?

9. What is the transfer rate of a eight-track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per second?

10. How many 1024 × 1 RAM chips are needed to provide a memory capacity of 16 K bytes?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Describe the representation of floating point number in the computer. (8)

(ii) Explain the common bus system constructed with multiplexers and three-state buffers. (8)

Or

(b) (i) Discuss the different instruction formats with example. (8)

(ii) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer. (8)

12. (a) (i) Explain the microprogrammed control unit with neat block diagram. (8)

(ii) A computer has 16 registers, an ALU with 32 operations, and a shifter with eight operations, all connected to a common bus system. (8)

(1) Formulate a control word for a microoperation.

(2) Specify the number of bits in each field of the control word and give a general encoding scheme.

(3) Show the bits of the control word that specify the microoperations $R4 \leftarrow R5 + R6$.

Or

(b) (i) Discuss the different addressing modes with example. (8)

(ii) Explain the major characteristics of RISC processor. (8)

13. (a) (i) Derive an algorithm in flowchart form for the non-restoring method of fixed point binary division. (8)

(ii) Explain the Booth's multiplication algorithm. Give the Booth's multiplier for 1100110101111. (8)

Or

(b) (i) Formulate a four segment instruction pipeline for a computer. Specify the operation to be performed in each segment. (8)

(ii) Explain the function of vector processor. (8)

14. (a) (i) Explain the DMA controller with neat diagram. (8)

(ii) Design a 4 × 4 FIFO buffer for asynchronous data transfer and explain its operations. (8)

Or

(b) (i) Explain different modes of data transfer between peripherals. (8)

(ii) A CPU with 20-MHz clock is connected to a memory unit whose access time is 40 s. Formulate a read and write timing diagrams using a READ strobe and a WRITE strobe. Include the address in the timing diagram. (8)

15. (a) (i) Explain the different mapping methods used in cache memory in detail. (8)

(ii) An 8 bit computer has a 16 bit address bus. The first 15 lines of the address are used to select a bank of 32 K bytes of memory. The high order bit of the address is used to select a register that receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32 K bytes each., for a total of 256 K bytes of memory. (8)

Or

(b) (i) Explain with block diagram how multiple matched words can be read out from an associative memory. (8)

(ii) Explain the paging process performed in virtual memory in detail. (8)
