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M.E DEGREE EXAMINATIONS: JANUARY 2011

First Semester

APPLIED ELECTRONICS

ANE501: Advanced Digital System Design

Time: Three Hours **Maximum Marks: 100**

Answer All Questions:-

PART A (10 x 2 = 20 Marks)

1. Differentiate Mealy and Moore Models.
2. Illustrate the timing of an Algorithmic State Machine.
3. What are essential hazards? Explain.
4. Describe the purpose of IPAC.
5. Differentiate PAL and PLD.
6. Create a PLD description for 2 x 4 multiplexer.
7. Name the various faults that can occur in PLA.
8. What is a test vector? Explain.
9. Explain compilation and simulation of VHDL code.
10. Write the VHDL code for binary full adder.

PART B (5 x 16 = 80 Marks)

11. a) For the state tale shown in Table 1, obtain the clocked synchronous sequential circuit using T flip flop.

Table 1

Present State		**Next State**		**Output (z)**	
A	B	X=0	X=1	X=0	X=1
		A_{n+1} B_{n+1}	A_{n+1} B_{n+1}		
0	0	0 0	0 1	0	0
0	1	1 1	0 1	0	0
1	0	1 0	0 0	1	1
1	1	1 0	1 1	0	0

(OR)

b) (i) Construct an ASM chart for a counter that can have 4, 6 or 8 states. The type of counter is decremented by checking two input variables x_1 and x_2, when the counter is

in its first state and should remain in the same state as long as $x_1 = x_2 = 0$ and as mod-4 counter when $x_1 = 1$ and $x_2 = 0$, as mod-6 counter when $x_1 = 0$ and $x_2 = 1$ and mod-8 counter when $x_1 = 1$ and $x_2 = 1$. A single output z is asserted only during last state of the counting sequence. (10)

(ii) Develop the ASM Chart for a binary multiplier. (6)

12. a) Design an asynchronous sequential circuit that has two inputs $x_1$and x_2 and a single output z. The output is to remain as 0 as long as x_1 is a 0. The first change in x_2 occurs while x_1 is 1 will cause z to be 1. Z remains in 1 until x_1 returns to 0.

1. Construct a timing diagram to represent input and output changes.
2. Construct a state diagram and flow table.
3. Reduce the flow table.
4. Draw the logic diagram and test the circuit.

(OR)

b) Design an asynchronous controller for a vending machine. A single slot is provided that will accept nickels, dimes and quarters. Each coin value is to be considered as a separate input variable. Products are available at two prices \$45 and \$55 with separate output for each price. When either output is reached a product select button is pushed and the machine resets.

13. a) (i) Realize the following Boolean equation with PLA with equivalent logic diagram.

$$x = abcd' + a'b'c + a,\ y = ab' + c'd,\ z = c + ab'.$$ (8)

(ii) Design a synchronous Modulo-8 binary counter using an EPROM to realize the combinational portion of the circuit. (8)

(OR)

b) (i) Realize a 4-bit adder using a PAL device. (8)

(ii) Explain how EPROM can be used to realize a sequential circuit. (8)

14. a) With an example show that the conventional Boolean difference method cannot derive tests for all internal nodes and can be solved using partial Boolean difference method.

(OR)

b) (i) Discuss on the different faults that can occur in PLA. (8)

(ii) Explain compact algorithm with an example. (8)

15. a) Draw the block diagram and write a VHDL description of a decimal counter that uses two of the above counters to form a two-decade decimal up/down counter that counts up from 00 to 99 or dowm from 99 to 00.

(OR)

b) (i) Write a note on the different VHDL operators. (8)

(ii) Model an SR Flip flop using VHDL (8)

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