M.E DEGREE EXAMINATIONS: JUNE 2011

Second Semester

APPLIED ELECTRONICS

ANE504: Analysis and Design of Analog Integrated Circuits

Time: Three Hours   **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 2 = 20 Marks)

1. Draw the small signal model of MOS Transistor and define each parameter.

2. Find the drain current and transconductance for a NMOS Transistor operating with

   V_{GS} =   2.5V, Vt= 1V, K_n =1mA/V^2

3. What is the need for startup circuit in a self biased V_{be} referenced current source

4. What is the main difference between current source and current sink?

5. List the various non ideal effects which can degrade the performance of practical op-amp

6. What is the significance of trimming technique in the design of low drift op-amp?

7. State the need for compensation in an op-amp

8. Give two important features of a cascode amplifier

9. Draw the circuit of simple emitter coupled pair multiplier

10. What is the use of phase comparator in a PLL?

PART B (5 x 16 = 80 Marks)

11. a) Derive an expression for the Depletion layer depth and small signal capacitance of a
       PN Junction

(OR)

   b (i) Analyze the working of MOS transistor in the various regions of operation   (8)

   (ii) Explain the short channel effects in MOS transistor   (8)

12. a) Explain Bipolar Widlar current source and find its output current and using the small
       signal model, derive its output resistance

(OR)

   b) (i) Explain in detail supply independent biasing methods   (10)

   (ii) Draw and explain the transfer characteristics of Push pull output stage   (6)

13. a) (i) Explain in detail about the DC Analysis of 741 op-amp (10)

(ii) Analyze the bias circuitry of 741 op-amp (6)

(OR)

b) Write short notes on

(i) Dominant pole and non dominant pole of 741 (8)

(ii) Noise model of Op-amp (8)

14. a) (i) Explain the operation of a Wilson MOS current mirror and derive the expression for

r_{out} and V_{min} (8)

(ii) Compare the performance of various MOS current mirrors (8)

(OR)

b) (i) Explain in detail the Miller compensated two stage CMOS operational amplifier and

its bias circuitry (8)

(ii) Discuss the frequency response of an operational amplifier (8)

15. a) (i) Determine the DC Transfer characteristics of a Gilbert Multiplier cell (8)

(ii) How Gilbert cell is used as an analog multiplier with two different approaches to

increase the input signal range (8)

(OR)

b) (i) With block diagram explain the PLL system (6)

(ii) Perform the closed loop analysis of a first order phase locked loop and describe the

operation with necessary waveforms (10)

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