

M.E. DEGREE EXAMINATIONS: JUNE 2011

Second Semester

APPLIED ELECTRONICS

ANE505: Computer Architecture and Parallel Processing

Time: Three hours

Maximum Marks: 100

Answer ALL Questions

PART A (10x2 = 20 Marks)

1. What is tightly coupled System?
2. List the Flynn's Classification?
3. What is Hit Miss ratio?
4. What is meant by backplane bus?
5. List any two latency hiding techniques.
6. What is the advantage of Worm hole routing over Store and forward routing?
7. What is saturation and Linear region in Multi threaded processor operation?
8. Define the order of memory events?
9. What are the essential requirements for Critical Section in Shared variable programming model?
10. What type of operating system adopted in UNIX?

PART B (5 x 16= 80 Marks)

11. a) (i) Explain the Flynn's classification of computer Architectures in detail (8)
(ii) Explain the VLSI Complexity model for processor array. (8)
- (OR)**
- b) (i) Explain the different Speed up performance Laws (8)
(ii) Explain the grain packing and scheduling with example (8)
12. a) (i) Explain the Architecture of vector super computer with neat diagram (8)
(ii) Calculate the access time of main memory and capacity of disk array for effective access time= 10.04 μ s with cache and main memory hit ratio of 0.98 and 0.9

respectively. The maximum cost of the memory hierarchy should be Rs 15000. The memory hierarchy specifications are.

Level	Access time	Capacity	Cost/Kbyte
Cache	25 ns	512 Kbytes	Rs 1.25
Main Memory	?	32 Mbytes	Rs 0.2
Disk Array	4 ms	?	Rs 0.0002

(OR)

- b) (i) Explain the properties Inclusion, Coherence and Locality used in memory Hierarchy.
(ii) Explain the different mapping techniques used in cache memory organization.

13. a) (i) Explain the various classifications of pipeline processors. (8)
(ii) Discuss the problems to be considered while designing instruction pipelines. (8)

(OR)

- b) (i) Explain any one dynamic interconnection networks with examples. (8)
(ii) Explain Backplane bus system. (8)

14. a) Explain different types of dataflow machine architecture

(OR)

- b) What is meant by Compound Vector function? Consider the execution of following

$$\text{CVF: } A(I)=B(I)/C(I)+D(I)*E(I) + F(I) - G(I).$$

Show all the stages in PIPENET development for the pipelined execution of CVF

15. a) Explain with various examples(Commands) from UNIX, justify it is highly suitable for multiprocessing requirement.

(OR)

- b) Enlist and explain the features required for parallel programming environment with parallel operation model.
