Register No: ……

M.E DEGREE EXAMINATIONS: JUNE 2011

Second Semester

APPLIED ELECTRONICS

ANE507: ASIC Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 2 = 20 Marks)

1. Draw the ASIC design flow.
2. Define effort delay.
3. Draw the static RAM diagram.
4. What is metastability?
5. List out the low-level design languages.
6. What is PIA?
7. What is logic synthesis?
8. What is the use of “Configuration” in VHDL?
9. Define fault coverage.
10. What are the types of fault?

PART B (5 x 16 = 80 Marks)

11. a) Explain the different types of ASIC design methodologies.

(OR)

b) What are the different sequential logic cells used in ASIC? Explain with example.

12. a) (i) Explain the two types of antifuse. (10)

(ii) What is PREP? Mention the benchmark circuits of PREP (6)

(OR)

b) An ASIC implementation requires that the design to be fused permanently. Also the design uses fine grained structure. Choose an appropriate P-ASIC and justify the selection.

13. a) Describe the Xilinx LCA interconnect architecture.

(OR)

b) Explain the schematic entry method of ASIC design with necessary diagram.

14. a) Explain with example how the following are synthesized in VHDL.

(i) Initialization and reset

(ii) Multiplexers

(iii) Combinational Logic Synthesis

(iv) Adders

(OR)

b) Explain the steps involved in synthesis of sequential logic in VHDL.

15. a) What are the different types of simulation? Explain with example.

(OR)

b) Explain the built in self test.

****