Register No: ……..

B.E. DEGREE EXAMINATIONS: APRIL/MAY 2011

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U07EC604: Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 1 = 10 Marks)

1. The third state of the three state bus buffer is _____

A) low impedance B) high impedance C)low inductance D)high inductance

2. The shift micro operations for R ← shr R refers to _____

A) shift right register R B) circular shift resister R

C) arithmetic shift register R D) shift left register R

3. For a _____ operation, different Levels of partial results have to be added repeatedly.

A) add B) subtract C) multiply D) divide

4. A divide overflow occurs if

A) high order bits of the dividend greater or equal to divisor

B) low order bits of the dividend greater or equal to divisor

C) high order bits of the divisor greater to dividend

D) low order bits of the divisor greater to dividend

5. The cache memory access time is less than the access time of main memory by a factor of

A) 10 -15 B) 15-20 C) 0-5 D) 5-10

6. An address used by a programmer will be called a _____

A) Physical address B) Memory space C) Virtual address D) Logical address

7. The highest level of memory hierarchy of a computer system is assigned to _____

A) Register file B) RAM C) ROM D) Magnetic Tape

8. Each word in the control memory contains within is a _____

A) Micro program B) Micro instruction C) Mini program D) Mini instruction

9. A _____ causes the interface to respond by transferring data from bus into one of the registers

A) Control command B) Status command C) Data output command D) Data input command

10. The _____ input is used by the DMA controller to request the CPU to relinguish control of the buses

A) Bus request B) Bus grant C) Bus response D) Bus transfer

PART B (10 x 2 = 20 Marks)

11. Define integer representation
12. List out the arithmetic micro operations
13. What is divide overflow?
14. What is dividend alignment?
15. Define memory address space.
16. Define content addressable memory
17. Differentiate between microinstruction and micoprogram.
18. What is pipelining?
19. Define polling
20. What is handshaking?

PART C (5 x 14 = 70 Marks)

21. a) Explain in detail about the Logical micro operations

(OR)

b) Explain in detail about Shift micro operations.

22. a) (i) Explain the operation of a BCD Adder/Subtractor circuit in detail. (7)

(ii) Write short notes on BCD subtractor? (7)

(OR)

b) Illustrate Booth algorithm with an example.

23. a) Explain in detail about the cache memory.

(OR)

b) Explain in detail about the virtual memory.

24. a) Explain micro programmed control unit and what are the advantages and disadvantages of it?

(OR)

b) Explain in detail about instruction pipeline and its Hazards.

25. a) Explain the DMA controller with neat diagram.

(OR)

b) Explain in detail about the Asynchronous data transfer.

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