Register Number: ……..

B.E DEGREE EXAMINATIONS: NOV/DEC 2012

Third Semester

ECE103: DIGITAL ELECTRONICS

(Common to CSE, ECE, MCE, IT)

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. A group of four binary digits is called
   a) Word b) Byte
   c) Nibble d) Long Word
2. The main application of Excess-3 code is in
   a) 2's Complement arithmetic b) Binary Subtraction
   c) BCD Subtraction d) Code conversion
3. One of the following is a universal gate -
   a) AND b) NOT
   c) EX-OR d) NAND
4. A group of 4 adjacent 1's in a K-map is called
   a) Nibble b) Quad
   c) Octet d) Pairs
5. The main drawback of ripple carry adder is
   a) High power dissipation b) Complex circuitry
   c) High propagation delay d) Slow response time
6. In a half-subtractor, difference could be realized using the gate -
   a) AND b) NAND
   c) NOR d) EX-NOR
7. 'Modulo' in a n-bit counter represents
   a) Number of bits b) Maximum value
   c) Number of states d) Minimum value
8. The essential hazard is avoided by
   a) Adding feedback b) Adding delay elements
   c) Edge triggering d) Using master-slave configuration
9. In a standard TTL, the sink current, I_{OL}, is typically
   a) -16 mA b) -1.6 mA
   c) +5 mA d) 4.8 mA
10. The main advantage of CMOS over TTL is

a) Higher speed
b) Low fan-out
c) Low power dissipation
d) High current drive

PART B (10 x 2 = 20 Marks)

11. What is a reflex code? Give an example.
12. Convert the binary word, '1010' into Gray code.
13. State the equation for 'sum' output of a full adder.
14. Compare de-multiplexor and decoder.
15. Draw the truth table for edge-triggered JK Flip-Flop.
16. What is a synchronous circuit?
17. What are the characteristics of Mealy model?
18. What are hazards? List any two types of hazards.
19. State the salient features of ECL family.
20. What is the structure of PLA?

PART C (5 x 14 = 70 Marks)

21. a) (i) State DeMorgan's laws. Prove them using Truth-Table. 4

(ii) Simplify using K-map, given a system described by Boolean equation, 10
$y = \sum m (7,9,10,11,12,13) + d(14,15)$

(OR)

b) (i) State Boolean Duality theorem. Explain with an example. 4

(ii) Simplify using Quine McClusky method the system defined by the Boolean equation, $y = \sum m (0,1,2,3,10,11,12,13,14) + d(15)$ 10

22. a) (i) Explain the four possible cases of 2's complement subtraction with examples. 8

(ii) Design and construct 4-bit parity generator. 6

(OR)

b) (i) Design and construct a 4-bit carry look-ahead adder.

23. a) Design and construct a Master-Slave JK Flip-Flop and explain the operation. Draw the truth-table.

(OR)

b) Draw the state sequence diagram for a mod-6 synchronous counter. Design and implement using JK flip-flop. Use state-table and also K-map for simplifying equations for output. Draw the final circuit.

24.	a)	(i)	Compare Mealy and Moore models.	4
		(ii)	Design and construct a asynchronous decade counter. Implement the design using JK Flip-flops.	10
			(OR)	
	b)		Using schematic, describe the working of a 4-bit universal shift register.	
25.	a)	(i)	How are memories classified? Describe the features of each.	7
		(ii)	Draw the circuit of a basic CMOS cell. Explain the working of the same in brief	7
			(OR)	
	b)	(i)	What are the main features of FPGA? Use a simple schematic describe the basic architecture.	7
		(ii)	Explain the architecture of PLA. Using a simple example, explain how PLA could be used for implementing combinational logic design.	7

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