Register No: ……

B.E. DEGREE EXAMINATIONS: NOV / DEC 2012

Fifth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE111: Digital Signal Processing

Time: Three hours **Maximum Marks: 100**

Answer all questions

PART A (10 x 1 = 10 Marks)

1. Let x (n) = δ(n).Then 4 point DFT of x (n) is

   a) {1,1,1,1} b) {1,0,0,0} c) {1,0,1,0} d) {0,0,0,1}

2. The circular convolution is known as

   a) aperiodic convolution b) linear convolution

   c) periodic convolution d) nonlinear convolution

3. Coefficient symmetry is important in FIR filters because it provides

   a) a smaller transition bandwidth b) less passband ripple

   c) less stopband ripple d) a linear phase response

4. A DSP convolves each discrete sample with four coefficients and they are all equal to 0.25. This must be an

   a) High pass filter b) Low pass filter c) Band pass filter d) Band stop filter

5. IIR filters

   a) Use feedback b) are sometimes called recursive filters

   c) can oscillate if not properly designed d) all of the above

6. _____ realization is less sensitive to process of quantization.

   a) Direct form I b) Direct form II c) Cascade d)Parallel

7. The output of two digital filters can be added. Or, the same effect can be achieved by

   a) adding their coefficients

   b) subtracting their coefficients

   c) convolving their coefficients

   d) averaging their coefficients and then using a Blackman window

8. If the R is the range of analog quantity to be quantized and b is the binary word size then quantization step size is

   a) R/2b b) R/2 c) 2R/ b d) $R/2^b$

9. The basic process that's going on inside a DSP chip is
a) quantization b) MAC c) logarithmic transformation d) vector calculations

10. The TMS320C67xx DSP uses

a) a floating -point digital signal processor with two-level cache-based architecture

b) a floating-point digital signal processor with three-level cache-based architecture

c) a fixed-point digital signal processor with two-level cache-based architecture

d) a fixed-point digital signal processor with three-level cache-based architecture

PART B (10 x 2 = 20 Marks)

11. Compute the DFT of sequence $x(n)=\{-2,2,1,-1\}$
12. Find the total number of multiplications required to compute 64-point FFT using radix-2 algorithm.
13. Write the necessary and sufficient conditions for the linear phase of an FIR filter.
14. State the advantages and disadvantages of FIR filter over IIR filter.
15. What is pre-warping in filter design?
16. Determine the order of the analog Butterworth filter that has a -2 db pass band attenuation at a frequency of 20 rad/sec and atleast -10 db stop band attenuation at 30 rad/sec.
17. Write the expression for signal to quantization noise ratio and calculate the improvement with an increase of 4 bits to the existing bits.
18. What do you mean by limit cycle oscillations in digital filter? What are the types of limit cycle oscillation?
19. List the factors that influence the selection of DSPs
20. Explain the concept of pipelining in DSP processor.

PART C (5 x 14 = 70 Marks)

21. a) (i) Compute the output of linear filter described by $h(n)=\{1,2,3,2,1\}$ and input $x(n)=\{1,1,1,1\}$ using DFT. (8)

(ii) From first principles, obtain the signal flow graph for computing 4-point DFT using radix-2 decimation-in-time FFT algorithm. (6)

(OR)

b) Determine the 8-point DFT of $x(n)=\{1,1,1,1,1,1,1,0\}$ using DIF-FFT algorithm.

22. a) Derive the expression for frequency response of a linear phase FIR filter with N- odd symmetric impulse response.

(OR)

b) The desired response of a LPF is

$$H_d(e^{j\omega}) = \begin{cases} (e^{-j3\omega}) & -0.75\pi \le \omega \le 0.75\pi \\ 0 & 0.75\pi \le |\omega| \le \pi \end{cases}$$

Determine $H(e^{j\omega})$ for M= 7 using Hamming window

23. a) Design a digital chebyshev filter Using bilinear transformation to satisfy the constraints

$$0.707 \le |H(e^{j\omega})| \le 1, \qquad 0 \le \omega \le 0.2\pi$$
$$|H(e^{j\omega})| \le 0.1, \qquad 0.5\pi \le \omega \le \pi$$

(OR)

b) Determine the direct form II cascade and parallel realizations for the system described by the system function y(n)=(3/4)y(n-1)-(1/8)y(n-2)+x(n)+(1/3)x(n-1).

24. a) (i) What is truncation error? Discuss its effect on all types of number representation? (8)

(ii) What is the effect of quantization on pole locations? (6)

(OR)

b) In a cascaded realization of the first order digital filter, the system function of the individual section are $H_1(z) = 1 / (1-0.9\ z^{-1})$ and $H_2(z) = 1 / (1-0.8z^{-1})$. Draw the product quantization noise model of the system and determine the output noise power.

25. a) Explain the architecture and important features of Digital Signal Processor TMS320C54XX

(OR)

b) Describe the various addressing modes of Digital Signal Processor TMS320C67XX.

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