Register Number……

B.E., DEGREE EXAMINATIONS: NOV/DEC 2012

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE119: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer All Questions:-

PART A (10 x 1 = 10 Marks)

1. The distance between nmos and pmos transistor is determined by
   a) Minimum separation between p+ active area and p well.
   b) Minimum separation between n+ active area and n well.
   c) Minimum separation between n+ active area and p well.
   d) Minimum separation between p+ active area and n well.

2. Which of the following is true for an nmos transistor operating in its *linear* or *triode* mode?
   (Vgs = gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)
   (a) Vds < (Vgs - Vt) (b) Vds > (Vgs - Vt)
   (c) Vgs < Vt (d) Vgs = 0v

3. When a MOS device is in saturation, the effective channel length ---------- when Vds increases
   a) Decreases b) Increases c) Does not vary d) Varies randomly

4. In Lambda-based design rule, the value of λ is ---------
   a) 0.001 µm b) 0.01 µm c) 0.1 µm d) 1.0 µm

5. Switches formed used transmission gate comprises of
   a) Simple n-pass transistor b) n-pass and p-pass in parallel
   c) Simple p-pass transistor d) n-pass and p-pass in serial

6. Transmission gates degrades ---------- logic
   a) Both 0 and 1 b) Neither 0 nor 1 c) Only 0 d) Only 1

7. One of the programmable ASIC is
   a) F PGA b) PLA c) PLC d) PAL

8. The difference between a PLA and a PAL is:
   a) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.
   b) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
   c) The PAL has more possible product terms than the PLA
   d) PALs and PLAs are the same
9. @ (clock) a = b; is
   a) Delay-based timing control statement b) Event-based timing control statement
   c) Level-Sensitive timing control statement d) Macro statement
10. Which of the following is used for verilog-based synthesis tools?
   a) Intra-statement delay statements can be synthesized, but inter-statement delays cannot
   b) Inter-statement delay statements can be synthesized, but intra-statement delays cannot
   c) Initial values on the wires are always ignored
   d) Synthesized results are identical for 'if' and 'case' statements.

PART B (10 x 2 = 20 Marks)

11. List the different types of CMOS process.
12. Define threshold voltage.
13. Draw the stick diagram of CMOS inverter
14. Mention the limitation of scaling of MOS devices.
15. What is domino CMOS logic?
16. Give the advantage of using Pass transistor logic.
17. Draw the Xilinx FPGA architecture.
18. What are the different methods of programming of PALs?
19. What are the two blocks in behavioral modeling? Explain.
20. Compare blocking and non-blocking assignment in verilog.

PART C (5 x 14 = 70 Marks)

21. a) (i) Describe in detail step-by-step procedure of CMOS fabrication process. (8)
   (ii) Compare CMOS and BICMOS technologies. (6)

(OR)

b) (i) Discuss clearly the SOI fabrication process. (8)

(ii) Explain the operation of PMOS enhancement transistor. (6)

22. a) Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.

(OR)

b) (i) Discuss the method of latch-up prevention in CMOS circuits (7)

(ii) With neat diagram, explain lamda-based design rules for contact cuts and vias. (7)

23. a) (i) Show that the pseudo-nMOS logic determines the required ratio of $\frac{Z_{p.u.}}{Z_{p.d.}} = \frac{3}{1}$. (8)

(ii) Compare static and dynamic CMOS logic Circuits. (6)

(OR)

b) (i) Design 4:1 MUX using transmission gates. (6)

(ii) Explain the dynamic two bit shift register circuit using NMOS and CMOS logic. (8)

24. a) (i) Describe the programmable logic structure available in PAL. (7)

(ii) Explain the finite state machine design using PLA. (7)

(OR)

b) Explain the FPGA design flow with neat diagram. Enumerate clearly the different steps involved.

25. a) (i) Write a verilog program for 3 to 8 decoder in gate level description. (8)

(ii) Describe the concept of gate delay in verilog with an example. (6)

(OR)

b) (i) Explain the concept involved in structural gate level modeling and also give the description for half adder. (8)

(ii) Write a note on back end tools. (6)

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