Register Number: ……..

B.E., DEGREE EXAMINATIONS: NOV/DEC 2012

Seventh Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

EIE117: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. CMOS technology is better than bipolar technology because

   a) High noise margin. b) Low packing density.

   c) Low input impedance. d) High output admittance.

2. The distance between drain and source diffusion regions is called as

   a) Channel width. b) Channel length.

   c) Channel d) Subthreshold region

3. What is the minimum metal width in layout design rule?

   a) 1λ b) 2 λ

   c) 3 λ d) 4 λ

4. How do you create zero threshold transistors?

   a) need extra ionization step b) need extra oxidation step

   c) need extra masking step d) need extra oxidation step

5. Barrel shifter is used in the hardware implementation of

   a) ALU b) Control unit

   c) Floating point arithmetic d) Shift register

6. Which clocking system eliminates race and hazard problem/

   a) Single phase clocking system b) two- phase clocking system

   c) gated clock d) three- phase clocking system

7. A NOR-NOR realization of an NMOS PLA used with

   a) Enhancement mode pull up device b) Depletion mode pull down device

   c) Enhancement mode pull down device d) Depletion mode pull up device

8. The content of a single programmable logic device consists of

a) fuse link arrays
b) thousands of basic logic gates
c) advanced sequential logic functions
d) thousands of basic logic gates and advanced sequential logic function

9. The data type used to implement a state machine in VHDL is

a) state
b) enumeration
c) Data
d) Logic

10. In VHDL, the mode of a port does not define

a) an input
b) an output
c) both input and output
d) the TYPE of the bit

PART B (10 x 2 = 20 Marks)

11. What is the special feature of Twin-Tub process?
12. What is Channel-stop Implantation?
13. Give the various color coding used in stick diagram
14. Define Pass transistor logic
15. Draw the clocked precharged high 2 input nMOS NAND gate
16. Design a set of CMOS gates to implement the sum of product function.
17. Define Mealy and Moore machine
18. Define FSM
19. What is the importance of operator precedence in VHDL?
20. What are basic design units of VHDL?

PART C (5 x 14 = 70 Marks)

21. a) (i) Clearly explain the body effect and channel length modulation of a MOS FET. (7)

(ii) Derive an equation for Ids of an n channel enhancement MOSFET. (7)

(OR)

b) (i) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET (7)

(ii) Explain the various steps in nMOS fabrication with neat diagrams. (7)

22. a) Derive the CMOS inverter transfer characteristics

(OR)

b) (i) Design a stick diagram and layout diagram for the CMOS logic shown below (7)

$$Y = \overline{(A + B)(C + D)}$$

(ii) Draw the following transistors using lambda based design rules: (7)
NMOS enhancement and PMOS enhancement type

23. a) (i) Explain the concept of dynamic CMOS design (10)

(ii) Explain the structure design of parity generator (4)

(OR)

b) (i) Define tally circuit. Design a 3 input tally circuit using pass transistor with suitable stick diagram (7)

(ii) Construct CMOS 4:1 MUX using pass transistor (7)

24. a) Draw and explain the pseudo-nMOS PLA schematic for full adder and what are the advantages and disadvantages of it.

(OR)

b) (i) With neat sketches explain the NAND-NAND structure of PLA (7)

(ii) Draw and explain the architecture of an FPGA (7)

25. a) (i) Explain how a FSM model is described in VHDL with suitable program. (7)

(ii) What is meant by Hierarchy in VHDL? Write a program for 4 input Multiplexer from 2 input multiplexers. (7)

(OR)

b) (i) Write a VHDL program in behavioral modeling with concurrent codes (7)

(ii) Write a VHDL program for 8 bit carry look ahead adder. (7)

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