Register Number……

M.E., DEGREE EXAMINATIONS: NOV/DEC 2012

Third Semester

EMBEDDED SYSTEMS

PED568: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer All Questions:-

PART A (10 x 2 = 20 Marks)

1. What is oxidation process?
2. List the advantages of SOI?
3. Define threshold voltage?
4. Draw transmission gate?
5. Define Sheet resistance and Area capacitance?
6. What is Latch up?
7. What is pass transistor?
8. Compare Dynamic CMOS Logic and Clocked CMOS Logic?
9. List the importance of CMOS testing?
10. What is built in self test?

PART B (5 x 16 = 80 Marks)

11. a) Explain NMOS Fabrication Technology with neat diagram?

(OR)

b) Write short notes on

(i) Twin tub process (8)

(ii) Silicon on Insulator (8)

12. a) Derive the basic DC equation of MOS transistor in all three operating regions?

(OR)

b) Explain in detail about the second order effects of MOS transistor?

13. a) With neat sketch explain the CMOS nwellpwell design rules?

(OR)

b) Write short notes on

(i) Wiring capacitance. (8)

(ii) Drive large capacitive loads. (8)

14. a) Draw and explain simple combinational logic design with any example?

(OR)

b) Discuss in detail about the CMOS Logic design with neat diagram?

15. a) With neat sketch explain the Boundary scan test of a system?

(OR)

b) (i) Explain IDDQ test? (8)

(ii) Write short notes on Built in self test? (8)

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