Register Number: …….

M.E DEGREE EXAMINATIONS: JUNE 2012

Second Semester

APPLIED ELECTRONICS

ANE504: Analysis & Design of Analog Integrated Circuits

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 2 = 20 Marks)

1. The collector-base leakage current of an *npn* transistor with the emitter open is given by 10^{-10}A at 24^{o}C.

   Estimate the value of collector-base leakage current at 120^{o}C. Assume the transistor is operating in forward active region. Neglect the surface leakage effects. Also comment on the significance of leakage current at high temperatures.

2. Draw the complete low frequency small-signal model for the circuit shown below. Assume the pMOS load transistor can be modeled by output resistance r_{o2}.

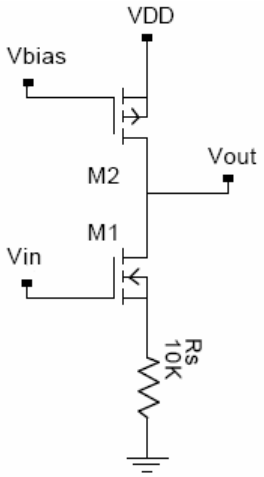

Figure1

3. Draw the circuit diagram of a current mirror with beta helper. Mention its significance.
4. What is bootstrap bias technique?
5. How drift is reduced in operational amplifiers?
6. List and explain at least two reasons to select a two-stage op amp with an n-channel input pair instead of with a p-channel input pair for a given application.
7. In the input stage of the 741 shown below in Figure2, calculate the collector currents in Q_{10} and Q_{13} when the supply voltage is $\pm$10V. Neglect the effects of finite output resistance in the transistors.

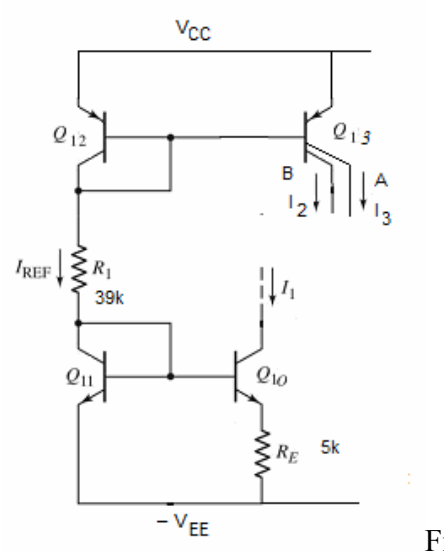

Figure2

8. What are the advantages and disadvantages of the common-source output stage?

9. Sketch the dc transfer curve I_{out} versus V_2 for the Gilbert Multiplier for $V_1=0.5V_T$.

10. List out various noise in integrated circuits.

PART B (5 x 16 = 80 Marks)

11. a) (i) A plane-abrupt *pn* junction in silicon has doping densities $N_A=8x10^{15}$ atoms/cm^3 and $N_D=10^{17}$ atoms/cm^3.

(a) Which side of the junction (*p* or *n*?) will have the majority of the depletion layer?

(b) Calculate the built-in potential, depletion-layer depths, and maximum field with 5 V reverse bias. Take $n_i=1.5x10^{10}$ cm^{-3} at 300^o K.

(c) Calculate the zero-bias junction capacitance and also calculate the value at 5 V reverse bias.

Assume junction area of $2x10^{-5}$ cm^2.

(d) Calculate the breakdown voltage for the junction, if the critical field is ε_{crit} = 4 $x10^5$ V/cm. (10)

(ii) Explain the dependence of transistor current gain β_F on operating conditions. Sketch the curves of β_F versus I_C for an integrated circuit transistor. Also state the reasons for the behavior of β_F with I_C. (6)

(OR)

b) (i) Explain short-channel effects in MOS transistors. (8)

(ii) Using the following data, derive the low frequency small signal model for an nMOS transistor in saturation.

$N_A=10^{15}$ (substrate), Vt=1 V, V_{DS}=3 V, V_{GS} =2 V, V_{SB}=1V, I_D=88□A, W=2mm, L = 1mm, □$_F$ = 0.35 V, μ_nCox = 80□A/V^2, λ = 0.05 V^{-1}, and γ = 0.5 V$^{1/2}$. (8)

12. a) Design an active load for an emitter coupled differential pair. Analyze the effect of active load on the output resistance and CMRR.

(OR)

b) (i) Derive the large-signal transfer characteristics of the emitter-follower output stage with current- mirror bias. Analyze the characteristic for different values of load resistance. (8)

(ii) A band-gap reference in bipolar technology is designed to give a nominal output voltage of 1.262V, which gives zero TC_F at 27^{o}C. Because of component variations the actual room temperature output voltage is 1.280V. Find the temperature of actual zero TC_F of V_{OUT}. Also express V_{OUT} as a function of temperature, and calculate the TC_F at room temperature. Assume γ=3.2 and α=1. (8)

13. a) (i) Explain the issues involved in designing a low drift and low input current operational amplifier. (8)

(ii) Determine the gain of the 741 if the bias current level in the input stage is doubled. (8)

(OR)

b) Draw the high frequency equivalent circuit of the 741 op-amp. Estimate the -3dB frequency and non-dominant pole.

14. a) Draw the schematic of a folded-cascode op amp. How it is different from the standard cascade configuration? Determine the output swing by choosing an appropriate current mirror. Calculate the voltage gain and output resistance. State the assumptions made.

(OR)

b) Design a MOS Widlar current source to meet the following constraints with V_{DD} = 3V;

(i) The input current should be 100□A, and the output current should be 10□A.

(ii) V_{ov1} = 0.2V

(iii) Transistor M2 must operate in the active region if the voltage from the drain of M2 to ground is atleast 0.2V.

(iv) The output resistance should be 50MΩ.

Ignore the body effect. Assume L_{drwn}=1 □m and Xd = Ld=0. Channel-length modulation parameter = 0.02 □m/V. Assume other parameters required.

15. a) (i) The ac schematic of an amplifier is shown in figure3. The circuit is fed from a current source i_s and data are as follows: R_S=1kΩ, R_L=10kΩ, I_C = 1mA, β=50, r_b=0, r_o=∞.

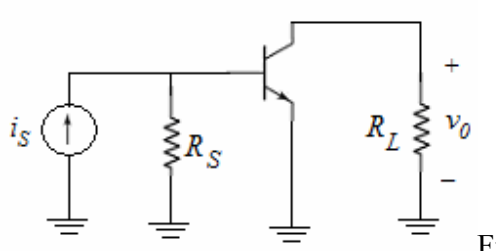

Figure3

Neglecting capacitive effects and flicker noise, calculate the total noise voltage spectral density at v_o in V^2/Hz. Thus calculate the MDS at i_s if the circuit bandwidth is limited to a sharp cut-off at 2 MHz. (10)

(ii) A phase-locked loop has a center frequency of 10^5 rad/s, a K_O of 10^3 rad/V-s, and a K_D of 1 V/rad. There is no other gain in the loop. Determine the loop bandwidth in the first-order loop configuration. Determine the single-pole, loop-filter pole location to give the closed-loop poles located on 45^o radials from the origin. (6)

(OR)

b) Show that the emitter-coupled pair can be used as a primitive multiplier. Modify the circuit to form a Gilbert multiplier cell. Perform dc analysis and derive the transfer characteristic to show that the circuit allows four-quadrant multiplication. Also show that the differential output current is proportional to the product of input voltages.

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