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V 4123

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2008.

Seventh Semester

(Regulation 2004)

Electrical and Electronics Engineering

CS 1034 — COMPUTER ARCHITECTURE

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Perform $11010 - 10000_2$ using 1's complement and 2's complement.

2. Define micro-instruction

3. What is a control memory?

4. What are the merits and demerits of Reduced Instruction Set Computer?

5. Define throughput and efficiency of a pipelined architecture.

6. List the characteristics of vector processing.

7. What are the needs for input and output interfaces?

8. What are the basic advantages and disadvantages of priority interrupt over a non-priority system?

9. How many 128 × 4 RAM chips are needed to provide a memory capacity of 2048 bytes?

10. What is meant by cache coherence problem?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. The output should be logic-1 when the inputs contain an unused combination in the code. (10)

(ii) Explain any six logic micro-operations in detail. (6)

Or

(b) (i) Name and explain various registers available in a typical computer system. (8)

(ii) What is the range of numbers that can be accommodated in a 16-bit register when the binary numbers are represented in Sign-magnitude and Sign-2's complement schemes? Give the answers in equivalent decimal representation. (8)

12. (a) (i) What is the difference between hard-wired control and micro-program control? What are the advantages and disadvantages in each method? (8)

(ii) With a neat diagram explain the organization of a typical micro-program sequencer. (8)

Or

(b) (i) What is meant by addressing mode? Explain various addressing modes in detail. (8)

(ii) Explain various instruction formats in detail. (8)

13. (a) (i) Show the hardware to be used for the addition and subtraction of two decimal numbers in signed-magnitude representation. Indicate how overflow is detected. (8)

(ii) Describe the key design problems of pipeline processors. (8)

Or

(b) (i) Describe the design of an arithmetic pipeline with an example. (8)

(ii) Derive the algorithm in flow chat form for the division of two floating-point numbers. (8)

14. (a) (i) Describe the functions of a typical asynchronous communication interface with a neat diagram. (10)

(ii) Explain the signals exchanged between the CPU and the DMA prior to the data transfer by the DMA. (6)

Or

(b) (i) Explain how priority for simultaneous interrupts is established using hardware approach. (10)

(ii) What programming steps are required to check when a source interrupts the computer while it is still being serviced by a previous interrupt request from the same source? (6)

15. (a) (i) Compare the relative merits and demerits of the following cache mechanism

Direct mapping cache

Fully associative mapping

Set associative mapping. (9)

(ii) Explain memory hierarchy in detail. (7)

Or

(b) (i) Explain how the virtual address is translated into real address in a paged virtual memory system. (10)

(ii) Explain the organization of a magnetic disk in detail (6)