

Reg. No. :

**V 4550**

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2008.

Fifth Semester

(Regulation 2004)

Computer Science and Engineering

CS 1304 — MICROPROCESSORS AND MICROCONTROLLERS

(Common to B.E. (Part-Time) Fourth Semester Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the interrupt signals present in 8085 processor in the priority order.
2. Give the sequence of operation that takes place during the execution of call instruction.
3. List the advantages of using segment registers in 8086.
4. How is allocation and pre-assignment of the structure directives done?
5. Explain the BHE and LOCK signals of 8086.
6. Explain why the processor utilization rate can be improved in a multiprocessor system by an instruction queue.
7. Describe the three major tasks needed to get meaningful information from matrix keyboard.
8. What are the different ways in which the 8-bit data bus of an interfacing device can be connected to the 16 bit data bus of 8086?
9. How does 8051 differentiate between the external and internal program memory?
10. Give the difference between the microprocessor and micro controller.

PART B --- (5 × 16 = 80 marks)

11. (a) (i) Draw the timing diagram for SHLD 16-bit address. (8)  
(ii) Write an 8085 ALP to convert hexadecimal value to decimal value (8)

Or

- (b) Draw and discuss the internal architecture of 8085 in detail.  
12. (a) (i) Discuss in detail the data related addressing modes of 8086 with an example. (10)  
(ii) Write an 8086 ALP to reverse a string. (6)

Or

- (b) (i) Discuss in detail the interrupts and interrupt service routine in 8086 processor. (8)  
(ii) Define a macro that produces code for adding two binary N-byte operands and storing the N-byte result beginning at an arbitrary location. N is to be the name of a constant and is to appear as the fourth dummy parameter. (8)  
13. (a) Draw and discuss the configuration diagram for the maximum mode operation of 8086. (16)

Or

- (b) Assume that a loosely coupled multiprocessor system consists of an 8086 with a local memory in one module and in another module two 8089's with a local I/O bus. Determine the major bus interface devices required for each module. (16)  
14. (a) Discuss how the DMA controller is interfaced with the 8085 processor. (16)

Or

- (b) Discuss in detail about the programmable interrupt controller and its cascading mode of operation. (16)  
15. (a) Discuss the register set of 8051 and also discuss how memory and I/O addressing is done in 8051. (16)

Or

- (b) Discuss in detail the internal architecture of an 8051 microcontroller (16)