Reg. No. : | | | | | | | | | | | |

V 4563

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2008.

Fifth Semester

(Regulation 2004)

Electrical and Electronics Engineering

EC 1312 — DIGITAL LOGIC CIRCUITS

(Common to B.E. (Part-Time) Fourth Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert $(427.24)_8$ to binary number.

2. State the associative law of Boolean algebra.

3. Write down the truth table of XOR gate. Give an application for XOR function.

4. Draw a 2 to 1 multiplexer using basic gates.

5. Draw the logic circuit of a clocked JK flipflop.

6. How many flip flops are required to design a mod-15 counter?

7. Define a combinational logic circuit. Give an example.

8. Define a sequential logic circuit. Give an example.

9. What is a PLA?

10. Define noise margin.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Prove the following Boolean identities. (8)

$x + xyz + yzx' + wx + w'x + x'y = x + y$

$(x_1 + x_2)(x_1' x_3' + x_3)(x_2' + x_1 x_3)' = x_1' x_2$

(ii) Simplify the following switching function

$f(x_1, x_2, x_3, x_4, x_5) = \sum m\,(1, 3, 6, 10, 11, 12, 14, 15, 17, 19, 20, 22, 24, 29, 30)$ (8)

Or

(b) Find the minimal SOP form for the following 6 variable switching function.

$f(x_1, x_2, x_3, x_4, x_5, x_6) = \sum m\,(2, 3, 6, 7, 10, 14, 18, 19, 22, 23,$

$27, 37, 42, 43, 45, 46, 58, 59)$

Implement the reduced function using NAND gates only.

12. (a) Design and implement a full adder circuit and a full subtractor circuit.

Or

(b) Design and implement a 8421 to gray code converter. Realize the converter using only NAND gates.

13. (a) Design and implement a synchronous decade counter. Explain its working. Draw the timing diagram.

Or

(b) (i) Explain the working of a master-slave JK flip flop. (6)

(ii) For a four bit even parity bit generator, inputs come serially. The four bits of the input sequence are to be examined by the circuit and circuit produces a parity bit which is to be added in the original sequence. The circuit should get ready for receiving another four bits after producing a parity bit for the last sequence. Draw the state diagram and write down the state transition table. (10)

14. (a) Design a pulse mode circuit having two input lines x_1 and x_2 and one output line z. The circuit should produce an output pulse to coincide with the last input pulse in the sequence $x_1\ x_2\ x_2$. No other input sequence should produce an output pulse.

Or

15.

(b) Design a two-input (x_1, x_2), two-output (z_1, z_2) fundamental-mode circuit that has the following specifications. When $x_1\ x_2 = 00, z_1\ z_2 = 00$. The output 10 will be produced following the occurrence of the input sequence 00-01-11. The output will remain at 10 until the input returns to 00 at which time it becomes 00. An output of 01 will be produced following the receipt of the input sequence 00-10-11. And once again, the output will remain at 01 until a 00 input occurs, which returns the output to 00.

15. (a) Write notes on :

(i) EPROM

(ii) PLD

(iii) PGA

(iv) ECL family.

Or

(b) (i) Explain the working of 2 input TTL totem-pole NAND gate circuit. (8)

(ii) Explain the working of 2 input CMOS NAND gate circuit. (8)