Reg. No. : ☐☐☐☐☐☐☐☐☐☐☐

T 3367

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2008.

Third Semester

Mechatronics Engineering

MH 1201 — DIGITAL ELECTRONICS

(Regulation 2004)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Subtract 278_{10} from 495_{10}.

2. Show that a positive logic AND gate is a negative logic OR gate.

3. How many select lines are required to design 32 line-to-1 line MUX?

4. A certain memory has capacity of 16K x 32. How many words does it store?

5. Give the block diagram of a PLA.

6. How will you convert a JK-FF in to a T-FF and D-FF?

7. What is an ASM chart?

8. Mention different types of memory decoding.

9. What do you understand by state reduction?

10. Differentiate between an internal state and a total state.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Convert the decimal number 250.5 to base 3, base 4, base 8, and base 16.   (8)

    (ii) Perform the following binary arithmetic operations :

        (1) $11111110_2 + 10101010_2$ and

        (2) $11111110_2 - 10101010_2$ (8)

Or

(b) (i) Prove the two canonical forms of a Boolean function. (8)

(ii) Simplify the Boolean function using Karnaugh map method.

$F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$

And the don't-care conditions :

$d(w, x, y, z) = \Sigma(1, 2, 5)$. (8)

12. (a) (i) Design a switching circuit that converts the 4-bit binary code into the 4-bit gray code using ROM array. (10)

(ii) Describe the function of a magnitude comparator. (6)

Or

(b) (i) Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number. (8)

(ii) Show how a full-adder can be converted to a full-subtractor with the addition of one inverter circuit. (8)

13. (a) (i) Compare combinational and sequential logic circuits. (8)

(ii) Draw the circuit of a 5-bit serial-in, serial-out shift register and explain. (8)

Or

(b) (i) Describe the array structure of $16\,K \times I$ dynamic RAM. (10)

(ii) List the advantages of dynamic RAM compared to static RAM. (6)

14. (a) (i) Investigate the transition table shown below and determine all race conditions and whether they are critical or non-critical. Also determine whether there are any cycles. (10)

	x_1x_2			
y_1y_2	00	01	11	10
00	10	00	11	10
01	01	00	10	10
11	01	00	11	11
10	11	00	10	10

(ii) Write a note on pulse mode sequential circuits. (6)

Or

(b) (i) Describe Hazards in combinational and sequential circuits. (8)

(ii) Find a circuit that has no static hazards and implements the Boolean function $F(w, x, y, z) = \Sigma(0, 2, 6, 7, 8, 10, 12)$ (8)

15. (a) Draw and explain an ASM chart for binary multiplier. (16)

Or

(b) Obtain the ASM charts for the following state transitions :

(i) If $x = 0$, control goes from state T_1 to state T_2 ; if $x = 1$, generate a conditional operation and go from T_1 to T_2.

(ii) If $x = 1$, control goes from T_1 to T_2 and then to T_3 ; if $x = 0$, control goes from T_1 to T_3.

(iii) Start from state T_1 ; then : if $xy = 00$, go to T_2 ; if $xy = 01$, go to T_3 ; if $xy = 10$, go to T_1 ; otherwise, go to T_3. (16)

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