Register Number.....

M.E. DEGREE EXAMINATIONS: DECEMBER 2008

First Semester

APPLIED ELECTRONICS

P07AE102 Advanced Digital System Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (20 x 1 = 20 Marks)

1. The main difference between the synchronous and asynchronous sequential circuit is the
   (a) clocking scheme applied (b) number of stages
   (c) inputs applied (d) combinational logic part

2. The main objective of the state assignment in the sequential circuit design is to reduce
   (a) the number of states
   (b) the combinational logic circuit
   (c) Clocking speed
   (d) the number of inputs and outputs

3. In ASM Chart
   (i) Output List is optional in state box
   (ii) Conditional output depends only on states and not on the inputs
   (a) True, False (b) True, True (c) False, False (d) False, True

4. Action Blocks in an ASM Chart represents
   (a) The blocks between two rectangle boxes
   (b) The blocks between two conditional outputs
   (c) The blocks between two branching boxes
   (d) The blocks between one rectangle box and conditional output

5. The Pulsed Mode and Fundamental mode are the classes of
   (a) Combinational Circuit (b) Synchronous Sequential Circuits
   (c) Asynchronous Sequential Circuits (d) Redundant Circuits

6. The table which lists the change of one state to the next state of circuit for a given input and output is the
   (a) Truth table (b) State Table (c) Transition Table (d) Excitation Table

7. F = (AB)' + AD is implemented using NAND logic. Find the hazard cover when A changes from 0 to 1 keeping B=D=1.
   (a) F = BD (b) F = B'D (c) F=BD' (d) F= B'D'

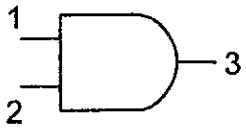
8. The following is the Hazards commonly found in Asynchronous Sequential Circuits

(a) Static 0 (b) Static 1 (c) Dynamic (d) Essential

9. In the following gate

(i) line 3 stuck at zero is equivalent to line 1 stuck at one and line 2 stuck at zero

(ii) line 3 stuck at one ,dominates line 1 stuck at one and line 2 stuck at zero

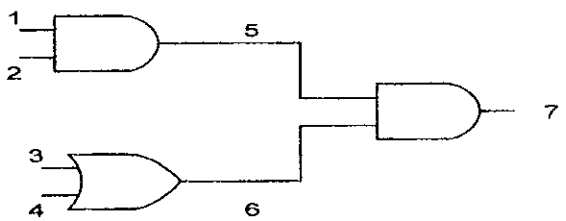


The above statements are

(a) (i) True (ii) True (b) (i) True (ii) False

(c) (i) False (ii) True (d) (i) False (ii) False

10. The test vector that detects the line 3 stuck at zero in the following logic circuit is



(a) 1110 (b) 1111 (c) 1101 (d) 1100

11. (i) A test t is said to distinguish between two faults f and g if $Z_f(t) \neq Z_g(t)$

(ii) For a single-output circuit, a test t that distinguishes between f and g makes $Z_f(t)$ $Z_g(t) = 0$

(Z is the logic function)

The above statements are

(a) (i) True (ii) False (b) (i) False (ii) False

(c) (i) False (ii) True (d) (i) True (ii) True

12. Consider a sequential network that has six inputs, one output and five states.

If the brute force approach is used to test the network, what will be the length of the input sequences and the total number of the test sequences required to test the circuit?

(a) 9 and 2^{54} (b) 10 and 2^{54} (c) 9 and 2^{25} (d)10 and 2^{25}

13. The programming technology used in Xilinx FPGAs

(a) Erasable EPROM (b) Erasable SRAM

(c) al-Polysilicon Antifuse (d) Metal-Metal Antifuse

14. In Xilinx 3000 FPGA

(i) The FGM Mode can realize functions of six or seven variables
(ii) The F Mode can generate two function of five variables
The above statements are

(a) True, True (b) False, False (c) True, False (d) False, True

15. A mask programmed PLD uses _____ technology

(a) CMOS (b) BiCMOS (c) SOI (d) BJT

16. Which of the logic array in a PLA device is programmable?

(a) Both AND and OR array (b) Only OR Array

(c) only AND array (d) None of the above

17. In VHDL _____ means "contents optional".

(a) :: = (b) { } (c) ( ) (d) [ ]

18. Block statements in VHDL are used to

(a) to enable signal drivers by using guards (b) to disable signal drivers

(c) to extend the scope of declarations (d) to block the declarations

19. _____ is a VHDL Data object

(a) Boolean (b) Variable (c) Physical (d) Access

20. (i) A bit_vector literal may be written either as a list of bits separated by commas ('1','0','1','1','0') or as a string "10110"

(ii) The formal-parameter-list in a function declaration is similar to that of a procedure, except parameters of class variables are not allowed.

The above statements are:

(a) True, True (b) True, False (c) False, False (d) False, True

PART B (5 x 16 = 80 Marks)

21. (a) Design a Clocked sequential circuit that produces the output sequence z for the input Sequence x as follows:

x = 001001000010010
z = 000100100001001

(OR)

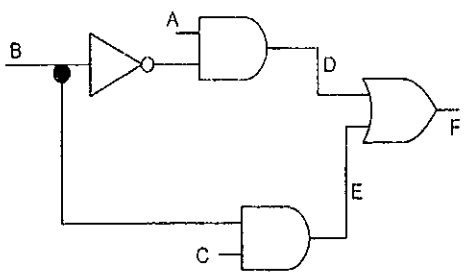
21.(b) For the given state transition table, produce a set of design equations for a minimal flip flop design. Realize the circuit and draw the ASM chart.

Present State [M N]		Next State [M,N]		Condition
A	0 0	B	01	True
B	0 1	C	10	True
C	1 0	A C D	00 10 11	X'Y' X'Y X
D	1 1	A B	00 01	Z Z'

22.(a) Design a Pulse-mode circuit having two input lines, x1, x2 and x3 and one output line, z. The Output must change from 0 to 1 if and only if the input sequence x1 – x2 –x3 occurs while Z = 0. The output must change from 1 to 0 only after an x2 input occurs.

(OR)

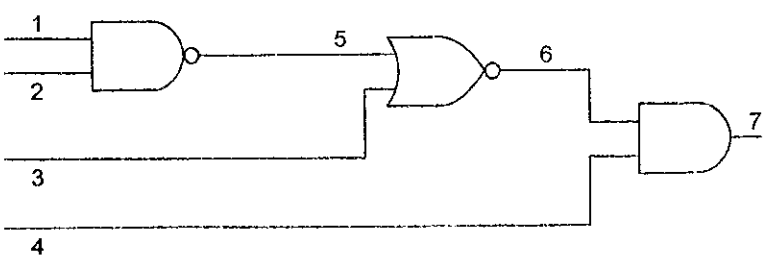
22.(b) In the Given Circuit assume that each gate has a propagation delay of 10 ns. Identify and explain the hazard present in this circuit by drawing the timing Chart. Also design the Hazard Free circuit.



23.(a) Derive the complete test set to detect the Single stuck at fault on line 2 using

(i) Path Sensitization method

(ii) Boolean Difference method



(OR)

23.(b) With an example explain the (i) Compact Algorithm and (ii) Kohavi Algorithm.

24.(a) With an example explain the PROM, PAL and PLA.

(OR)

24.(b) Compare and contrast the features of Xilinx 3000 and Xilin 2000 FPGAs

25.(a) Write the VHDL description in Structural Modeling for a BCD Counter

(OR)

25.(b) Write the VHDL Code in structural modeling for a

(i) 2x2 Multiplier

(ii) 3-bit parallel in serial out shift register.

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