M.C.A. DEGREE EXAMINATIONS: JANUARY – 2009

First Semester

P07CA101 COMPUTER ORGANIZATION

Time: Three Hours

Maximum Marks: 100

Answer All Questions:-

PART A (20 x 1 = 20 Marks)

1. Boolean Expression AB + A (CD + CD') can be simplified as

   A. A+ BC   B. A (B + C)   C. AD + B   D. AB + C D

2. An arithmetic expression (+42) + (-13) in binary using 2' complement form is

   A. 100010   B. 101001   C. 011101   D. 111000

3. The equivalent 4-bit excess-3 code of decimal number 15 is

   A. 1000 1001   B. 0100 1000   C. 1001 1111   D. 0001 0101

4. The output of the JK flip-flop is complemented, when J and K are

   A. 0 and 0   B. 0 and 1   C. 1 and 0   D. 1 and 1

5. How many 3 x 8 decoders are needed to construct a 5 x 32 decoder?

   A. 2   B. 3   C. 4   D. 5

6. A n bit binary counter is a register of n flip-flops and gates that follows a sequence of states from 0 to

   A. n   B. 2n   C. 2^n D. 2^n-1

7. What gate is used to perform both the addition and subtraction operations in a 4-bit adder-subtractor?

   A. NAND   B. NOR   C. XOR   D. AND

8. The combinational circuit used to construct a common bus system in a computer

   A. Decoder   B. Encoder   C. Multiplexer   D. Full Adder

9. The register that holds the address of the next instruction to be executed in a computer is

   A. Instruction Register   B. Program Counter   C. Address Register   D. Accumulator

10. During which time signal, the type of the instruction is determined in the instruction cycle.

    A. T0   B. T1   C. T2   D.T3

11. The pseudo instruction in an assembler informs the assembler about

    A. Symbolic Codes   B. Instructions   C. Operands   D. Translation

12. BSA instruction branches and saves the address of

    A. Current Instruction   B. Subroutine   C. Next Instruction   D. Operand

13. In memory mapped-I/O method, for memory and I/O access, computers use

    A. separate address   B. same address
    C. separate address and same instruction   D. same address and same instruction

14. Strobe is a

    A. Timing Signal   B. Source/Destination-Initiated Control Signal

    C. Source-Initiated Control Signal   D. Destination-Initiated Control Signal

15. DMA is used for data fast transfer between

    A. Memory and CPU   B. CPU and I/O Device
    C. Memory and I/O Device   D. RAM and ROM

16. UART is a

    A. Serial Port   B. Parallel Port   C. Serial and Parallel Port   D. Web Access port

17. Bootstrap program is loaded from

    A. RAM   B. ROM   C. Secondary Memory   D. Cache Memory

18. When Hit Ratio is high , the CPU accesses

    A. Cache more than Memory   B. Memory more than Cache

    C. Cache and Memory equally   D. Neither Cache nor Memory

19. The instruction PUSH is

    A. Zero-Address Instruction   B. One-Address Instruction

    C. Three-Address Instruction   D. Four-Address Instruction

20. The page fault occurs, when a page referenced by the CPU is in

    A. Not in Auxillary Memory   B. Not in Main Memory and Auxillary Memory

    C. Both   D. Not in Main Memory, but in Auxillary Memory

PART B (5 x16 = 80 Marks)

21. a) (i). Discuss on fixed point representation in computers. (8)

    (ii). Write on the binary codes a) Gray Code b) Weighted Code (8)

(OR)

21. b).(i) Simplify the following Boolean function in sum-of-products form by means of a four-variable map. Draw the logic diagram with a) AND-OR gates   b) NAND gates.

$$F(A,B,C,D) = \sum (0,2,8,9,10,11,14,15)$$ (11)

    (ii) Draw the state diagram for 2-bit binary counter and explain. (5)

22. a).(i) What is a multiplexer? Construct a 4-to-1 line multiplexer and explain its operation by means of a function table. (8)

    (ii) Draw the circuit of 4-bit shift register and describe its working principle.   (8)

(OR)

22. b). (i) The following transfer statements specify a memory. Explain the memory operation in each case. (6)

$$R2 \leftarrow M[AR]$$
$$M[AR] \leftarrow R3$$
$$R5 \leftarrow M[R5]$$

    (ii). Explain the functioning of Arithmetic Logic Unit with a diagram. (10)

23. a) State the phases of an instruction cycle and explain the process in each phase of the instruction cycle with a flowchart. (16)

(OR)

23. b).(i) Discuss on various basic registers in a computer. (8)

    (ii) Write an assembly language program to add two integer numbers. (8)

24.a). Explain in detail about the asynchronous data transfer in computers. (16)

(OR)

24. b) (i) What are the modes of data transfer to and from peripherals? (4)

    (ii) Discuss on CPU-IOP communication in I/O processor with a diagram. (12)

25.a). (i) Explain the organization of a stack in a computer and state its use. (8)

(ii) Discuss on various addressing modes used in an instruction format. (8)

(OR)

25. b).(i) What are data manipulation instructions? Give an example for each type of instruction. (5)

(ii) Explain the mapping procedures used to transform data from main memory to cache memory. (11)

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