Register Number.....

M.E. DEGREE EXAMINATIONS: DECEMBER 2008

First Semester

COMPUTER SCIENCE AND ENGINEERING

P07CS101 Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (20 × 1 = 20 Marks)

1. An enhanced CPU is 10 times faster on computation than the original processor. Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement.

   A. 15.6. B. 1.56 C. 2.56 D. 25.6.

2. The property that states that recently accessed items are likely to be accessed in the near future is called as

   A. Temporal locality
   B. Equidistant locality of reference
   C. Spatial locality
   D. Branch locality

3. Dynamic shared libraries uses,

   A. PC relative addressing mode
   B. Register direct addressing mode
   C. Register-indirect addressing mode
   D. PC-indirect addressing mode

4. The instruction used for performing dot product operations of vectors and matrix multiplies are called

   A. multiply accumulate instructions
   B. paired single operations
   C. partitioned add operation
   D. vector operation

5. The reason to allow structural hazard to occur is

   A. to reduce cost
   B. To reduce latency
   C. to reduce cost and latency
   D. it is not wise to allow structural hazard

6. The purpose of pipeline-interlock is

   A. to stall the pipeline until the hazard is cleared
   B. clears the data hazard
   C. perform data forwarding
   D. Allows pipeline to proceed ignoring the hazard

7. A non-pipelined has an overall CPI of 3.61 cycles/instruction and has clock cycle time of 25ns.How long does it take to run a program consisting of 857,000,000 instructions?

   A. 77.34 seconds B. 7.73 seconds C. 7.17 seconds D. 71.7 seconds

8. Speculation is a technique

   A. to avoid control dependence stalls
   B. to avoid structural stalls
   C. to monitor instruction execution
   D. Does not avoid any hazard

9. Which of the following is true?

A. Register renaming and jump prediction eliminate all control dependences
B. Branch and jump prediction eliminates all control dependences
C. Branch and jump prediction eliminates all true data dependences
D. Branch and jump prediction eliminates structural dependence

10. The prediction scheme that uses profile history of program to make predictions is

A. Tournament based branch prediction
B. static branch prediction
C. perfect branch prediction9-stage pipeline
D. standard 2-bit prediction

11. WAW hazards are eliminated using

A. Out of order execution
B. speculation
C. Register renaming
D. Branch prediction

12. The desktop oriented processors

A. prefers ILP rather than Thread level parallelism.
B. Exploits the advantages of Thread level parallelism.
C. Does not look for parallelism in their operations
D. employs both ILP and Thread level parallelism in their operations

13. Thread level parallelism is achieved in

A. SIMD multiprocessor
B. MIMD multiprocessor
C. SISD multiprocessor
D. MISD multiprocessor

14. The average access time of a 64KB direct-mapped cache, if hit time is 1 clock cycle and the miss rate is 1.4% and the miss penalty is 75ns is

A. 2.05 ns B. 20.5 ns C. 25.3 ns D. 2.53 ns

15. Allowing reads and writes to complete out of order and using synchronization to enforce ordering is called

A. Sequential consistency
B. Relaxed consistency
C. Coarse-grained multithreading
D. Fine grained multithreading

16. The Cray T3DIE computers use

A. Distributed shared memory architecture
B. Symmetric shared memory architecture
C. Asymmetric shared memory architecture
D. Centralized common memory architecture

17 The reciprocal of mean time to failure is

A. mean time to repair
B. the rate of errors
C. the rate of failure repairs
D. the failure rate

18. Distributed block interleaved parity is

A. RAID-4 B. RAID-3 C. RAID-5 D.RAID-6

19. An I/O system with a single disk gets on average 50 I/O requests per second. Assume that the average time for a disk to service an I/O request is 10 ms. The utilization of the I/O system is

A. 0.5 B.0.05 C. 5 D. 50.

20. The time from the reception of the response until the user begins to enter the next Command is called

A. Entry time B. Think time C. System response time D. Transaction time.

PART-B (5 x 16= 80 Marks)

21. (a).(i) Explain in detail about the classification of instruction set architecture

(OR)

21. (b) (i) Discuss in detail about the addressing modes for control flow operations. (8)

(ii) Write sort notes on encoding an instruction set. (8)

22. (a) Explain how data hazard is overcome using dynamic scheduling

(OR)

22.(b) . (i) What is loop level parallelism? Explain how it is detected and enhanced (8)

(ii) Explain briefly about software pipelining. (8)

23. (a) What is ILP?Discuss in detail about various limitations of ILP.

(OR)

23.(b) (i) Write short notes on software and hardware speculation. (8)

(ii) Discuss briefly about thread level parallelism (8)

24. (a) Explain the working of Directory-based cache coherence protocol with state transition diagram.

(OR)

24. (b) Explain the memory consistency models in detail.

25.. (a) (i) Explain the various RAID levels with their advantages and disadvantages. (8)

(ii) Discuss briefly about Little queuing theory. (8)

(OR)

25. (b) Explain the various techniques used for cache miss rate reduction

****