Reg. No. : | | | | | | | | | | | |

H 2161

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2009.

Third Semester

Mechatronics Engineering

EC 154 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write down the truth table of NAND logic.

2. Write the two's and one's complement of 10110110.

3. Give one application each for a decoder and a comparator.

4. How many address lines are needed to access a 1024 × 8 RAM.

5. What is a sequential circuit?

6. Draw an appropriate circuit using JK flipflop to realise a T flipflop.

7. How many flipflops are necessary at the minimum to realise a mod-13 counter?

8. What is meant by races?

9. What is an algorithmic state machine?

10. What is a PLA?

PART B — (5 × 16 = 80 marks)

11. (a) (i) State and prove Demorgan's theorems. (8)

(ii) Minimise the following function using Karnaugh map

$f = \sum m\,(0, 1, 4, 5, 7, 9, 11) + \sum d\ (2, 13)$

Implement the minimised function using NAND gates only. (8)

Or

(b) Minimise the following function using Quine McClusky method. Implement the minimised function using 15

(i) NAND gates only

(ii) NOR gates only.

$f = \sum m\,(1, 3, 4, 6, 8, 10, 12, 13, 14) + \sum d\ (0, 15)$

12. (a) Design and implement (i) full adder (ii) half subtractor (iii) 2 to 1 MUX. (8 + 4 + 4)

Or

(b) (i) Write notes on various types of read only memories. (8)

(ii) Design and implement (1) Comparator (2) 1 to 2 demux. (4 + 4)

13. (a) (i) Design and explain the working of a decade counter. (10)

(ii) Draw the truth table of SR, D and T flip-flops. (6)

Or

(b) (i) Explain the working of a single RAM cell. What are static and dynamic RAMs. (8)

(ii) Explain the working of a serial-in serial out shift register. Using appropriate timing diagram. Give an application for the same. (8)

14. (a) (i) Explain the various types of hazards. (8)

(ii) Define the following :

(1) State (1)

(2) Stable state (1)

(3) Unstable state (1)

(4) Maximum compatible state (1)

(8) (5) Cycle (2)

(6) Pulse mode sequential circuit. (2)

Or

ly. (8) (b) Design and draw an asynchronous sequential circuit using SR latch with two inputs A and B and one output Y. B is the control input which, when equal to 1, transfers, the input A to output Y. When B is 0, the output does not change, for any change in input.

y method.

15. (a) Design a digital system with two flipflops E and F and one 4 bit binary counter B has flipflops B_1, B_2, B_3 and B_4. B_4 holds the MSB of the count. A start signal S initiates the operation by clearing the counter B and Flipflop F. The counter is then incremented by starting from the next clock pulse and continues to increment until the operations stop. Counter bits B_3 and B_4 decide the sequence of operations.

(i) If $B_3 = 0$, E is cleared to 0 and the count continues

o 1 MUX.

(8 + 4 + 4) (ii) If $B_3 = 1$, E is set to 1, then if $B_4 = 0$ the count continues, but if $B_4 = 1$, F is set to 1 on the next clock pulse and the system stops counting. Draw an ASM chart for the design.

Or

(8) (b) Explain how multiplexers can be used in Design. Use an example to explain.

(4 + 4)

(10)

(6)

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static and

(8)

ster. Using

same. (8)

(8)

(1)

(1)